

# 493.73 HPS transition board

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This functional specification covers the 493.73 HPS transition board for the multi-channel / multi-station Cobra VME product.

Greg Ness   Feb-3-00     revision 0.9

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## Table of contents

|                                      |           |
|--------------------------------------|-----------|
| <b>x.1 introduction</b>              | <b>3</b>  |
| <b>x.2 specifications</b>            | <b>5</b>  |
| <b>x.3 functional description</b>    | <b>7</b>  |
| <b>x.4 registers / address map</b>   | <b>13</b> |
| <b>x.5 processor code</b>            | <b>24</b> |
| <b>x.6 self test</b>                 | <b>29</b> |
| <b>x.7 diagnostics</b>               | <b>29</b> |
| <b>x.8 connections</b>               | <b>30</b> |
| <b>x.9 configuration</b>             | <b>35</b> |
| <b>x.10 why did they do that?</b>    | <b>36</b> |
| <b>x.11 timing diagrams</b>          | <b>37</b> |
| <b>x.12 list of related drawings</b> | <b>38</b> |

### **change log**

|           |            |                                                                                                                                                                                                                                                                                                                       |
|-----------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Feb-3-00  | rev. 0.9   | minor changes before product release<br>added change bars for changes since rev. 0.3A                                                                                                                                                                                                                                 |
| Oct-20-99 | rev. 0.5   | added: digital I/O bits<br>service LED<br>ability to monitor station intlk lines<br>pwr_fail interlock bit<br>updates to intlk drawing, see text before drawing<br>removed HSP intlk override bit<br>added register bit cheat sheet<br>Garamond to Times Roman font for better readability<br>added table of contents |
| Feb-9-99  | rev 0.3A   | tweaks to registers and processor code info                                                                                                                                                                                                                                                                           |
| Dec-9-98  | rev. 0.2A  | minor revisions after design review                                                                                                                                                                                                                                                                                   |
| Nov-25-98 | rev. 0.01A | initial document                                                                                                                                                                                                                                                                                                      |

# x.1 introduction

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The 493.73 HPS transition board plugs into the rear panel of the multi-channel Cobra VME chassis (493.10). It is a single wide module that provides the following features:

- control of an HPS using the low level HPS interface
- remote E stop
- E stop output for shut down of 3rd party equipment
- digital I/O (3 in, 1 out) for system functions (UPS monitoring, etc.)
- external service LED

## internal features

no processor

no RAM

no watchdog timer

no serial EEPROM

This board is designed to plug into the transition board bus which is driven from the VME I/O Carrier board and will appear in the VME address space thru the Carrier. The transition board bus is a simplified VME style interface configured as A10:D16 and a minimal number of control lines.

A slot select line from the Carrier will enable each transition board as required. This results in no address jumpers on the HPS transition board to set incorrectly.

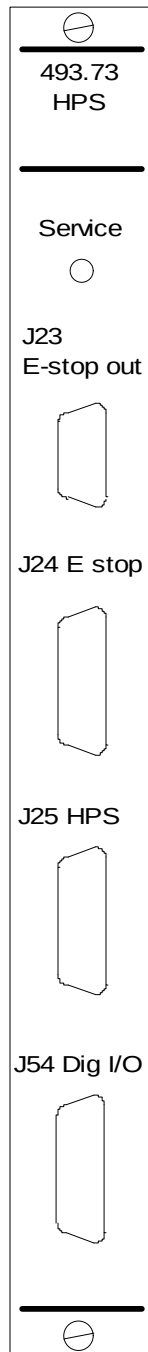
## HPS vs. HPU

Hydraulic Power Supply or Hydraulic Power Unit?

Some folks are starting to call this board the HPU board because most of the documentation for the units, er – pumps is being changed over from HPS to HPU.

front panel view

Below is a rough artist's conception of the front panel of the HPS transition board. Not to scale – well, duh.



## x.2 specifications

### 493.73 HPS transition board specifications

|                                           | PARAMETER                                         | SPECIFICATION                |
|-------------------------------------------|---------------------------------------------------|------------------------------|
| general                                   | power requirements                                |                              |
|                                           | 5 Vdc                                             | 0.1 A                        |
|                                           | ±12 Vdc                                           | none                         |
|                                           | ±15 Vdc                                           | none                         |
|                                           | 24 Vdc                                            | 0.03 A                       |
|                                           | power dissipation                                 | 1 watt typical, 2 watts max. |
|                                           | operating temperature range                       | 5-40°C                       |
|                                           | humidity                                          | 0-85%, non condensing        |
|                                           | altitude                                          | 10,000 ft max                |
|                                           | PWB size                                          | 233mm x 80mm (9.2" x 3.1")   |
| J25 HPS outputs (HPS start, low and high) | min drive current                                 | 10 mA into 2.2 k load        |
|                                           | max off state leakage                             | 4 µA (at 60°C)               |
| J25 HPS intlk inputs                      | max current draw                                  | 2 mA at 24 Vdc               |
|                                           | V <sub>OL</sub> max low voltage                   | 18.5 Vdc                     |
|                                           | V <sub>OH</sub> min high voltage                  | 23.1 Vdc                     |
| J25 HPS on sense input                    | max current draw                                  | 2 mA at 24 Vdc               |
|                                           | V <sub>OL</sub> max low voltage                   | 0.9 Vdc                      |
|                                           | V <sub>OH</sub> min high voltage                  | 5.5 Vdc                      |
| J24 E stop input                          | max voltage / current thru external E stop switch | 24 Vdc, 25 mA                |
| chassis E stop loop (J1 21a-22a)          | max voltage / current thru E stop loop            | 24 Vdc, 25 mA                |
| J23 E stop output                         | relay contact max voltage / current               | 24 Vdc or 24 Vac at 1 A      |
| J54 digital inputs                        | V <sub>IL</sub> max off voltage                   | 0.8 V                        |
|                                           | V <sub>IH</sub> min on voltage                    | 3.0 V at 0.3 mA              |

|                    |                                     |                                         |
|--------------------|-------------------------------------|-----------------------------------------|
|                    | max voltage                         | 26 Vdc at 3.8 mA                        |
|                    | input resistance                    | 6.6 k $\Omega$                          |
| J54 digital output | output format                       | open collector, open emitter transistor |
|                    | max voltage                         | 26 Vdc                                  |
|                    | min guaranteed output current drive | 20 mA (30 mA typical) at 1.0 V max      |
|                    | max output current without damage   | 80 mA                                   |
|                    | max output power dissipation        | 110 mW                                  |

## x.3 functional description

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### HPS

HPS control is done using the low level HPS interface which was pioneered on the 407 and 493.01 products. All control is done using 24 Vdc with a nominal current of 8 mA or less. The connector is a 15 pin D, identical to the 493.01 chassis (which is not the same as the high density 15 pin D used on the 407).

The usual HPS interlocks of low level and over temp are supported. Dirty filter is not supported since it is usually only provided on larger HPS's which aren't usually controlled directly from a 493 or similar controller.

which pumps can it be connected to?

Direct connection can be made to 24 Vdc HPS's that are compatible with the low current interface. This exclusive list includes these pumps:

- any 505 series pump (first units released in Jan-99)
- 506.52, .62, .72, .82 and .92 (24V versions only)

Connection to other older HPS's or any 115 V HPS requires the use of the 493.07 HPS converter box.

A 493.07 HPS converter box is required for connecting to any 512 HPS. This is because the 512 pumps have 115Vac on the E stop circuit and the HPS board can't handle 115V on the HPS D connector.

Since this product uses the same HPS interface and connector as the 493.01, the same HPS cable(s) can be used. For cable part numbers refer to the Cobra multi-channel system cable selector drawing (the 493.01 cable selector drawing (493359-01, [http://dodsun.mts.com/dsk2/493/49335901\\_sht2.pdf](http://dodsun.mts.com/dsk2/493/49335901_sht2.pdf)) can be used until the multi-channel selector drawing is available). For information on connecting multiple control panels of different vintages (407, 458, etc.) to a single HPS see the HPS compatibility guideline memo (<http://intranet.mts.com/users/n/nessg/hyd/hpsinfo.pdf>).

### E stop

A connector for a remote E stop box/switch is provided. It will always be 24V and low current (25mA max.). This eliminates the need for 18 AWG cable and a chassis ground wire as are needed if the E stop circuit could be 115 Vac (as on 458, 490, etc.).

As always there are 2 inputs provided on the E stop connector, a local interlock that is acted on by the controller and an input that goes back to the HPS for a redundant shut down. An E stop switch breaks both circuits when actuated.

On the HSM transition boards, connecting to only the local interlock circuit will generate a station stop that will shut down only a single station. Since the HPS board isn't assigned to any single station it doesn't have that option. The 2 circuits on the remote E stop are the HPS E stop circuit and a global interlock line. The global interlock line (for lack of a better description) will drive all station interlock lines active and stop the HPS but will not break the E stop output contact.

A remote E stop button must break both circuits on the remote E stop connector. A global stop button must break only the global interlock circuit.

The reason for having a 2<sup>nd</sup> input on the E stop input (in addition to the HPS E stop circuit) isn't to have a marginally useful global interlock available, the benefit is allowing the E stop switch to be monitored locally.

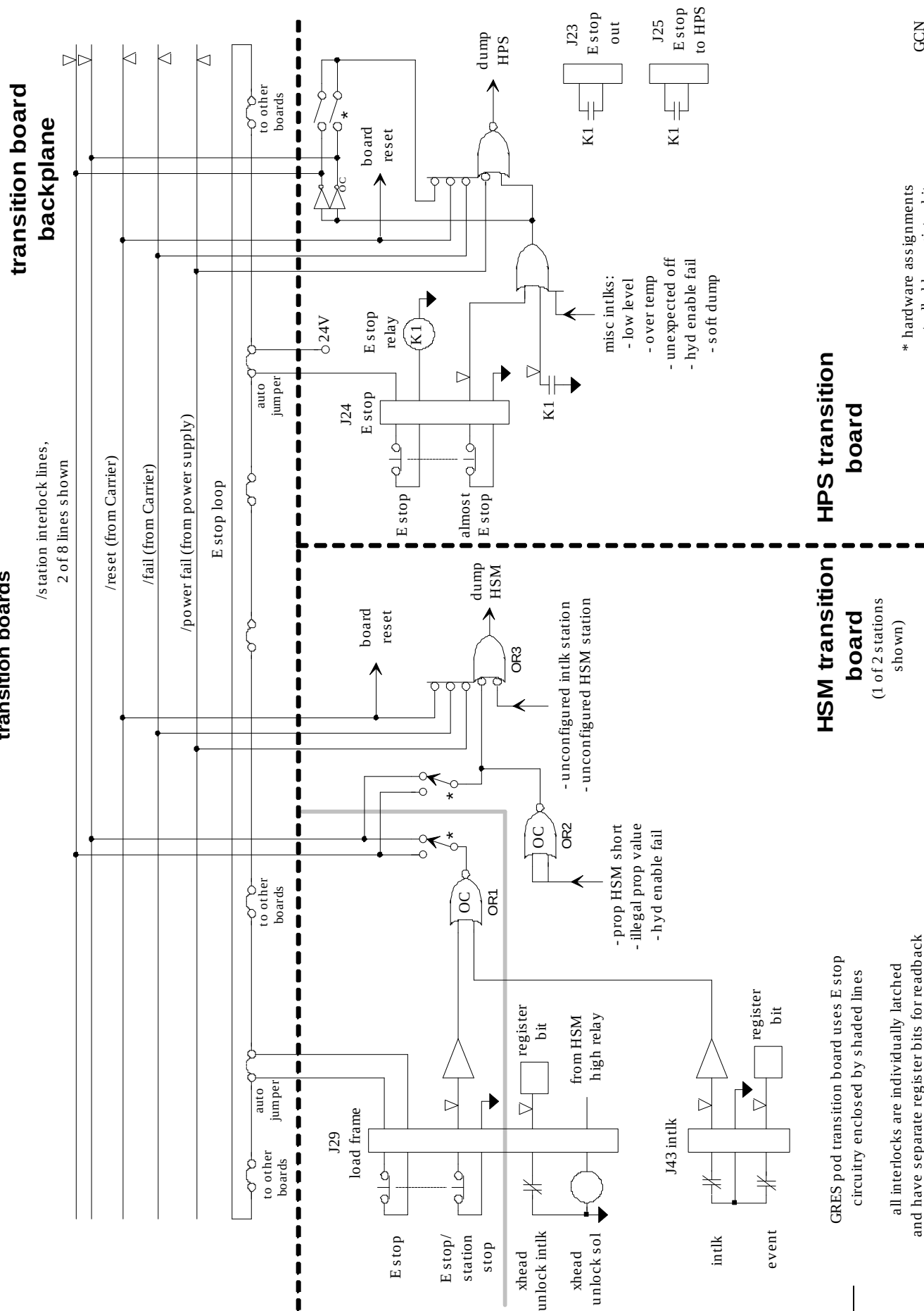
The HPS transition board buffers the E stop from the HPS with a relay. This provides a known low voltage and current to the E stop chain on the transition bus backplane. It also allows the HPS board to easily monitor the state of E stop from any board.

The drawing on the next page shows the interlock functionality of the HSM and HPS transition boards along with the transition backplane.

The interlock drawing was updated on Oct-21-99 and Dec-8-99 with these changes, most of which have been in place for a while:

- ◆ added power fail line on backplane (was always in hardware)
- ◆ deleted 24V fail detector on HSM board, now tied to power fail on backplane
- ◆ added station intlk monitoring (SW controlled) to HPS board, part of change request approved Sep-20-99
- ◆ listed hydraulic enable intlk on both boards (was always in the hardware)
- ◆ listed illegal proportional HSM values intlk on HSM board (was always in hardware)
- ◆ added 3rd OR gate on HSM board for interlocks and did rearranging of interlocks to keep interlocks associated with the HSM from the interlock OR gate (OR1) to one of the HSM OR gates (OR2 and OR3)

## multi-station Cobra interlocks transition boards



GRES pod transition board uses E stop  
circuitry enclosed by shaded lines

all interlocks are individually latched and have separate register bits for readback

\* hardware assignments controlled by register bits

## E stop out

This relay contact output allows external equipment to be shut down in unison with the Cobra VME box during an E stop. An E stop on any of the E stop buttons connected to the Cobra chassis will activate this output. Any station stop buttons will NOT activate the E stop output relay.

All of the E stop inputs on the HSM, HPS, pod or any other boards will break the E stop loop on the transition board backplane. The E stop out relay is driven by this loop so it responds to any E stop conditions in the entire chassis. Another contact on this relay breaks the E stop loop from the HPS in the event of an E stop.

The E stop output is NOT useable with 115 Vac due to the use of a D connector and PWB spacing limitations.

The relay driving the E stop output is normally energized. When an E stop occurs, or chassis power is off, the relay turns off. This means that the normally closed output is actually normally open and the normally open output is actually normally closed. Or something like that.

## digital I/O

The HPS board now contains 3 digital inputs and 1 digital output. These were added on the rev. B boards in Oct-99 before the release to production. These are a system level resource and they aren't tied to any station. The typical use is for monitoring an UPS.

All digital inputs are debounced for use with mechanical switch contacts.

The digital output is the transistor of an opto-isolator (or is that opto-coupler ???). The digital outputs are cleared to 0 when the fail line on the backplane is active.

## service LED

Also added on the rev. B prototypes in Oct-99 is a front panel service LED. It has the same functionality as the service LED on the 493.01 Cobra 1 chassis. It will be on after power up and will typically go off when the PowerPC makes contact with the host PC. This LED is completely under software control.

## number of HPS boards in a system

standard, supported configurations (1 HPS board per system)

In order for E stop to function correctly and shut down all stations, all systems must have exactly 1 HPS board. The HPS board may be located in any slot in the transition backplane. An E stop on any board will be seen by the HPS board and will generate an E stop.

A HPS board may be used with or without a HSM board.

The connectors used on the transition board backplane have switches that complete the E stop loop if there is no board installed in a slot. No jumper cards are needed. All transition boards must jumper across the E stop pins on the backplane connector if E stop is not used on that board.

don't even *think* about doing this (less than 1 HPS board)

If there is no HPS control in a system, it is possible to run the hardware without an HPS board. This will result in all of the E stop inputs acting only as station stop inputs, which will shut down only a single station. This does not meet the CE requirements for E stop and could be dangerous.

don't even *think* about doing this, either (more than 1 HPS board)

Using more than 1 HPS board in a system does not appear to be practical or possible for these reasons:

The system software probably won't support more than 1 HPS board. (Then again...)

The E stop loop on the backplane will be divided into 2 separate loops. Which boards are in which loop would be determined by the placement of the HPS boards. An E stop will be seen by only 1 of the HPS boards.

Any E stop will shut down all stations because the HPS board drives all station interlock lines active on an E stop. However, the other HPS won't shut down because it won't see the E stop (it won't even see a bunch of station interlocks because the HPS board generally doesn't monitor the station interlock lines).

It might be possible to have the software shut down all HPS's if all of the stations are shut down. However, this does NOT meet the definition of E stop in the machinery safety directive (EN 60204-1, 1992, section 9.2.5.4 "Where a category 0 stop is used for the emergency stop function, it shall have only hardwired electromechanical components." This is a category 0 stop.)

And the number 1 reason why more than 1 HPS board shouldn't be used in a system: The boss says so. (Explanation – if people reading the spec are given a glimmer of hope that they can run more than 1 HPS board in a system, someone will sell it and we will have to make it work. This will be a big problem for the reasons listed above. The system wasn't intended to accommodate more than 1 HPS board.)

## internal stuff

The HPS board is controlled with registers that are accessed from VME address space via the Carrier board. The Carrier board provides A10:D16 access to each transition board slot. Multiple slot select lines from the Carrier eliminate the need for address switches on any transition board.

### interlocks

Refer to the multi-station Cobra interlock diagram (several pages back) for a view of how the interlocks on the HPS and HSM transition boards fit in with the rest of the system. Briefly, the HPS board contains the E stop relay, which is monitored via one of the relay contacts. If the E stop relay drops out, all station lines are driven active to make sure that all HSM's get dumped.

Any of the HPS interlocks (low level, over temp and unexpected off) will also shut down the HPS and all stations.

Note that the HPS board drives all of the station interlock lines active only for some of the interlocks seen on the HPS board. It doesn't drive the station interlock lines for interlocks that are visible to all boards on other backplane lines (fail, power fail and reset). Refer to the interlock block diagram for details.

The HPS board can optionally monitor 1 or more of the station interlock lines and shut down the HPS if they go active. This could be used in a system without an HSM or HSM board where it's necessary to have the HPS shut down based on other interlocks in the system.

### programmable logic

The logic for the operation of the board is contained in an Altera EPLD (electrically programmed logic device). It is in circuit programmable using an Altera BitBlaster or ByteBlaster download cable, which connects to an internal 10 pin header.

## x.4 registers / address map

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### software identification of transition boards

Each slot select line on the transition board backplane will have a weak pull down on the Carrier (or the transition board backplane). Each transition board will have a strong pull up on the slot select line. A register on the Carrier will allow the state of these lines to be read back. A 0 will indicate an open slot and a 1 will indicate an installed transition board.

Alternatively, an attempt could be made to talk to each transition board slot. The lack of a response from any empty slot will generate a BEER (burp).

Each board will have a board ID register at the first address location. This will allow the software to determine the type of board in each slot.

### transition board addressing

There are no address select jumpers on the transition boards. Their address is determined by the slot position in the backplane. A separate slot select line from the I/O Carrier board is routed to each slot.

The I/O Carrier board determines the VME addresses and address modifiers used to access the transition bus.

Below is a table of the registers on the HPS transition board. The addresses listed must be added to the offset due to the slot address (dependant on the transition bus slot) and also to the base address on the I/O Carrier board.

Only 6 out of the 10 transition bus address bits are decoded on this board. This means that images of these registers will appear at addresses that are multiples of 0x80. Other addresses will NOT return a DTACK and will generate a bus error. (Was 5 address lines on rev. A prototypes.)

The architecture of the transition bus supports only D16 transfers.

Below is an equation that details how to determine the VME address of a particular transition board register given the I/O Carrier base address, the transition bus slot number and the transition board address (from the table in the next section). This assumes that the transition boards are on 64k address boundaries (even though the transition bus uses only 10 address lines).

$$\text{VME\_address} = \text{Carrier\_base} + (0x10000 * \text{slot\_number}) + \text{address}$$

Accesses to addresses not listed in the table below will NOT generate a DTACK and will be terminated with a bus error. (This wasn't implemented on the rev. A boards, but has been added on rev. B. Bad address = no DTACK)

All addresses are in hex.

## address map

**493.73 HPS transition board register address map**

| REGISTER               | ADDRESS<br>(HEX) | READ/<br>WRITE | WIDTH<br>(BITS) | INITIAL<br>VALUE |
|------------------------|------------------|----------------|-----------------|------------------|
| board ID               | 00               | R              | 16              | 0x0052           |
| HPS register           | 02               | R/W            | 16              | 0                |
| interlock register     | 04               | R              | 16              | *                |
| control register       | 06               | R/W            | 16              | 0                |
| digital I/O register   | 08               | R/W            | 16              | 0                |
| station intlk register | 0A               | R/W            | 16              | 0                |

\*The interlock register will power up with some combination of the current latched state of the interlocks and plain garbage. It must be cleared before starting hydraulics (the same as on existing products).

This section contains information on the individual register bits with a short description of each bit. Details on the interactions between different bits and specific procedures (clearing interlocks, etc.) are described in the next section (processor code).

Unused register bits read back as 0. They may be written with any value.

## board ID register

This read only register reads back a unique ID number to let the software determine what board is installed in each transition board slot.

**board ID register (addr 00)**

| BIT  | NAME     | FUNCTION |
|------|----------|----------|
| 0-15 | board ID | 0x0052   |

## HPS register

This register controls the outputs to the HPS

| HPS register (addr 02) |              |                                                              |
|------------------------|--------------|--------------------------------------------------------------|
| BIT                    | NAME         | FUNCTION                                                     |
| 0                      | HPS start    | 0 = HPS start output inactive<br>1 = HPS start output active |
| 1                      | HPS low      | 0 = HPS low output inactive<br>1 = HPS low output active     |
| 2                      | HPS high     | 0 = HPS high output inactive<br>1 = HPS high output active   |
| 3                      | HPS on sense | 0 = HPS is off<br>1 = HPS is on (or starting)                |
| 4-15                   | unused       | reads back as 0                                              |

Bits 0-2 control the 3 HPS outputs that drive the HPS.

(0) The HPS START bit starts the HPS.

(1) The HPS LOW bit holds the HPS in the on state.

(2) The HPS HIGH bit switches the HPS between low and high pressure.

(3) The HPS ON SENSE bit indicates whether or not the HPS is latched in the on state. This bit is read only, any value may be written.

The operation of the HPS register is the same as on the 493.01 Europa board.

Bits 0-2 are cleared by hardware when the HPS board sees any interlock. This includes all interlocks listed in the interlock register, but does not include any interlocks on any station interlock lines (unless enabled by setting bit(s) in the station mapping register).

The HPS is switched off by clearing bits 0-2.

For further information, refer to the processor code section of this spec, section x.5

## interlock register

All of the interlock sources for the HPS board have an individual bit in the interlock register, below. Any active interlock will shut down the HPS by clearing the bits in the HPS register and will drive all station interlock lines active (exception: the fail, power fail and reset lines on the backplane will not drive the station interlock lines).

Note that there is no lockout of interlocks in hardware. The software must keep track of which interlock occurred first. This allows the user to determine which interlock initiated the shut down when multiple interlocks become active during the shutdown. This is not a problem for the SW guys.

All interlocks are individually latched and are cleared by the CLR INTLK bit in the control register. An active interlock has priority over the CLR INTLK bit.

All external interlock inputs are debounced to allow use with mechanical contacts. The E stop and HPS interlocks are debounced with RC networks on the circuit board. The fail, power fail and station interlock inputs are debounced with a digital debounce circuit inside of the EPLD. See section 10 for more info.

### Important note about reporting interlocks

It is important that the software report a unique, descriptive error message for EACH active interlock – similar to the 493 system. This is a must for troubleshooting systems, both in house and in the field. Some older systems lumped many interlocks into a few categories and reported a vague error message (ie. controller interlock) which greatly hindered troubleshooting because much time was wasted trying to determine exactly which interlock is active.

It's true that the names of some of the obscure internal interlocks won't mean much to a customer or FSE, however, if/when they contact headquarters for additional assistance in solving a difficult problem, the description of the exact interlock that has been tripping will be invaluable.

### interlock register (addr 04)

| BIT | NAME               | FUNCTION                                                                     |
|-----|--------------------|------------------------------------------------------------------------------|
| 0   | HPS low level      | 0 = no interlock<br>1 = HPS low level interlock active                       |
| 1   | HPS over temp      | 0 = no interlock<br>1 = HPS over temp interlock active                       |
| 2   | unused             | reads back as 0                                                              |
| 3   | HPS unexpected off | 0 = no interlock<br>1 = intlk, unexpected HPS on to off transition detected  |
| 4   | fail               | 0 = no interlock<br>1 = backplane fail line interlock active                 |
| 5   | unused             | reads back as 0                                                              |
| 6   | hyd enable fail    | 0 = no interlock<br>1 = hyd enable interlock active                          |
| 7   | unused             | reads back as 0                                                              |
| 8   | chassis E stop     | 0 = no interlock<br>1 = E stop interlock active (chassis E stop loop broken) |
| 9   | unused             | reads back as 0                                                              |
| 10  | J24 E stop         | 0 = no interlock<br>1 = J24 E stop interlock active                          |
| 11  | unused             | reads back as 0                                                              |
| 12  | soft dump          | 0 = no interlock<br>1 = soft dump interlock active                           |
| 13  | pwr_fail           | 0 = no interlock<br>1 = backplane pwr_fail line interlock active             |
| 14  | station intlk      | 0 = no interlock<br>1 = backplane station intlk line interlock active        |
| 15  | reset /power up    | 0 = no interlock<br>1 = reset / power up interlock active                    |

(0) The HPS low level bit that indicates a low oil level at the HPS.

(1) The HPS over temp bit that indicates overheated oil in the HPS.

(3) This bit becomes a 1 when an unexpected HPS on to off transition happens on the HPS ON SENSE line *after the HPS has been latched on*. This would be due to the HPS shutting down for unknown external reasons, typically E stop at another controller or loss of power at the HPS. When this bit goes active it generates an interlock that will shut down the HPS control bits in the HPS register. DO NOT try to restart the HPS until the user presses the reset button and then the HPS LOW button.

- (4) Indicates the state of the FAIL line on the transition bus backplane.
- (6) This bit is active if a write is made to the HPS register before the HYD ENABLE bits (bits 4 and 5 in the control 1 register) are properly set up.
- (8) This bit will be active if the E stop loop on the transition bus backplane is broken. Any active E stop button will break this loop. This will drive an E stop out to the HPS and the E stop out connector. This bit can be used to differentiate between a station stop and an E stop. The station stop will not set this bit, where an E stop will set this bit.
- (10) The J24 E stop (or global interlock) bit will be active if the E stop switch connected to the J24 E stop connector on this board is pressed.
- (12) SOFT DUMP interlock line. It's generated by setting the SOFT DUMP bit in the Control register. It is used by software to dump hydraulics after a limit detect, error detect, etc.
- (13) The pwr\_fail interlock monitors the pwr\_fail line on the transition bus backplane. It's driven by the OR of all of the DC fail detectors on the power distribution board in the power supply.
- (14) Station interlock bit represents the debounced and latched station interlock line from the backplane. The station interlock lines can only generate an interlock if 1 or more bits are set in the station interlock mapping register, otherwise the station interlock lines are ignored.
- (15) Reset / power up interlock. It will be set at power up or when the reset line on the backplane is active. This interlock was added in Jan-99 to allow visibility for the case where the reset line on the backplane goes active and causes the hydraulics to shut down. Without this bit, the hydraulics would just appear to go inactive with no trace of what made it happen.

## control register

**control register (addr 06)**

| BIT   | NAME           | FUNCTION                                                                                |
|-------|----------------|-----------------------------------------------------------------------------------------|
| 0     | clear intlk    | 0 = inactive<br>1 = clear interlocks                                                    |
| 1     | unused         | reads back as 0                                                                         |
| 2     | soft dump      | 0 = inactive<br>1 = generate soft dump interlock                                        |
| 3     | unused         | reads back as 0                                                                         |
| 4     | hyd enable (L) | 0 = OK to write to HPS register<br>1 = write to HPS register will generate an interlock |
| 5     | hyd enable (H) | 0 = write to HPS register will generate an interlock<br>1 = OK to write to HPS register |
| 6     | unused         | reads back as 0                                                                         |
| 7     | unused         | reads back as 0                                                                         |
| 8     | unused         | reads back as 0 (used to be interlock override)                                         |
| 9     | unused         | reads back as 0                                                                         |
| 10    | unused         | reads back as 0                                                                         |
| 11    | unused         | reads back as 0                                                                         |
| 12    | service LED    | 0 = front panel service LED on<br>1 = LED off                                           |
| 13-15 | unused         | reads back as 0                                                                         |

(0) The CLR INTLK bit will clear all interlocks when a 1 is written. If an interlock is still active, the interlock will not be cleared. The CLR INTLK bit is not latched and will always read back as 0. It is not necessary to clear this bit after writing a 1.

(2) The SOFT DUMP bit is used by software to generate an interlock and dump hydraulics, typically after a limit detect or other error condition detected by the software. After this bit is set, it must be cleared by writing a zero before interlocks may be cleared.

(4, 5) These bits are used to enable writes to the HPS register. These bits must be set to 10(b) before hydraulics may be started (bit 5 = 1, bit 4 = 0). They are cleared to 00(b) at power up and after any interlock. If a write is attempted to the HPS register before the HYD ENABLE bits are enabled, an interlock will be generated (HYD ENABLE intlk).

This is a safeguard against runaway processors starting hydraulics by writing random data to random addresses. These bits must be set back to 10(b) after any interlocks are cleared. Clearing or changing the HYD ENABLE bits after hydraulics are started will not dump hydraulics. No action will be taken until a write to the HPS register is attempted.

(8) This bit is now unused. It was the HPS interlock override bit. But the HPS guys report that overriding HPS interlocks should only be done by the user when they are standing at the HPS, not at a remote control panel.

(12) Front panel service LED – At power up the bit is 0 so the LED is on. After the PowerPC makes contact with the host PC, the SW will turn the LED off – which is the same as on 493.01 Cobra 1. Other than the initial power up state, this bit is under software control.

## Digital I/O register

This register controls the digital inputs and outputs. The digital input bits are read only, any value may be written.

All inputs are debounced for use with mechanical contacts. The bits indicate the real time status of the digital inputs. There is NO transition detection or latching in hardware. Unconnected inputs will read as 0.

The digital output bit will be cleared if the backplane fail line goes active. The digital output is in the form of an opto-isolator (or is it opto-coupler ???) transistor.

**digital I/O register (addr 08)**

| BIT  | NAME      | FUNCTION                                                                                                  |
|------|-----------|-----------------------------------------------------------------------------------------------------------|
| 0    | dig in 1  | 0 = opto-isolator is off, external contact is open<br>1 = opto-coupler is on, external contact is closed  |
| 1    | dig in 2  | 0 = opto-isolator is off, external contact is open<br>1 = opto-isolator is on, external contact is closed |
| 2    | dig in 3  | 0 = opto-coupler is off, external contact is open<br>1 = opto-isolator is on, external contact is closed  |
| 3-14 | unused    | reads back as 0                                                                                           |
| 15   | dig out 1 | 0 = opto-coupler is off<br>1 = opto-isolator is on                                                        |

## HPS station interlock mapping register

This register controls which station interlock lines are monitored by the HPS board. The default is all bits off and the HPS board doesn't monitor any station interlock lines (same as the rev. A prototypes). If needed, 1 or more of these bits can be set which will dump the HPS when the associated station interlock line becomes active.

Most systems will leave these bits as all 0. The predicted main use is if a system doesn't contain an HSM or an HSM board, one of more of these bits can be set to make sure the HPS switches off in the event of a station intlk on any board.

### **WARNING: the currently planned software only supports up to 4 stations -or does it?**

As always, the HPS board will drive all station interlock lines active for any interlocks generated on the HPS board (HPS low level, over temp, E stop, etc.).

**HPS station mapping register (addr 0A)**

| BIT  | NAME      | FUNCTION                                                   |
|------|-----------|------------------------------------------------------------|
| 0    | station 1 | 0 = not mapped to station 1<br>1 = HPS mapped to station 1 |
| 1    | station 2 | 0 = not mapped to station 2<br>1 = HPS mapped to station 2 |
| 2    | station 3 | 0 = not mapped to station 3<br>1 = HPS mapped to station 3 |
| 3    | station 4 | 0 = not mapped to station 4<br>1 = HPS mapped to station 4 |
| 4    | station 5 | 0 = not mapped to station 5<br>1 = HPS mapped to station 5 |
| 5    | station 6 | 0 = not mapped to station 6<br>1 = HPS mapped to station 6 |
| 6    | station 7 | 0 = not mapped to station 7<br>1 = HPS mapped to station 7 |
| 7    | station 8 | 0 = not mapped to station 8<br>1 = HPS mapped to station 8 |
| 8-15 | unused    | reads back as 0                                            |

## 493.73 HPS board register cheat sheet

### register addresses

| REGISTER      | ADDR |
|---------------|------|
| board ID      | 00   |
| HPS           | 02   |
| interlock     | 04   |
| control       | 06   |
| digital I/O   | 08   |
| station intlk | 0A   |

### register bits

| BIT  | HPS      | INTERLOCK       | CONTROL             | DIGITAL I/O | STATION INTLK |
|------|----------|-----------------|---------------------|-------------|---------------|
| ADDR | 02       | 04              | 06                  | 08          | 0A            |
| 0    | start    | low level       | clear intlk         | dig in 1    | station 1     |
| 1    | low      | over temp       | -                   | dig in 2    | station 2     |
| 2    | high     | -               | soft dump           | dig in 3    | station 3     |
| 3    | on sense | unexpected off  | -                   | -           | station 4     |
| 4    | -        | fail line intlk | hyd enable (L)      | -           | station 5     |
| 5    | -        | -               | hyd enable (H)      | -           | station 6     |
| 6    | -        | hyd enable fail | -                   | -           | station 7     |
| 7    | -        | -               | -                   | -           | station 8     |
| 8    | -        | chassis E stop  | none (old override) | -           | -             |
| 9    | -        | -               | -                   | -           | -             |
| 10   | -        | J24 E stop      | -                   | -           | -             |
| 11   | -        | -               | -                   | -           | -             |
| 12   | -        | soft dump       | /service LED        | -           | -             |
| 13   | -        | power fail line | -                   | -           | -             |
| 14   | -        | station intlk   | -                   | -           | -             |
| 15   | -        | reset /power up | -                   | dig out 1   | -             |

Oct-18-99, for rev. B boards

## x.5 processor code

---

This section describes common procedures for banging the bits to perform specific functions (clearing interlocks, starting hydraulics, etc.). Refer to the register/address map section for specific information on all of the individual register bits.

### initial register setup

If necessary, the HPS board can be assigned to monitor 1 or more of the station interlock lines that will cause the HPS to dump if the selected interlock line(s) go active. This is done with the HPS interlock mapping register.

### clearing interlocks

Clear interlocks only once for each press of the interlock reset button. The interlocks will need to be cleared after power up.

- Write a 1 to the CLR INTLK bit in the control register (this bit is self-clearing and doesn't need to be written back to a 0).
- The interlock register will be 0x0000 (lemme see, that's 000 000 octal) if all of the interlocks are cleared. If 1 or more interlocks are still active, they will be set to 1 in the interlock register.

Note that there is no lockout of interlocks in hardware. The software must keep track of which interlock occurred first. This allows the user to determine which interlock initiated the shut down when multiple interlocks become active during the shutdown. This is not a problem for the SW guys.

An active interlock has priority over the CLR INTLK bit.

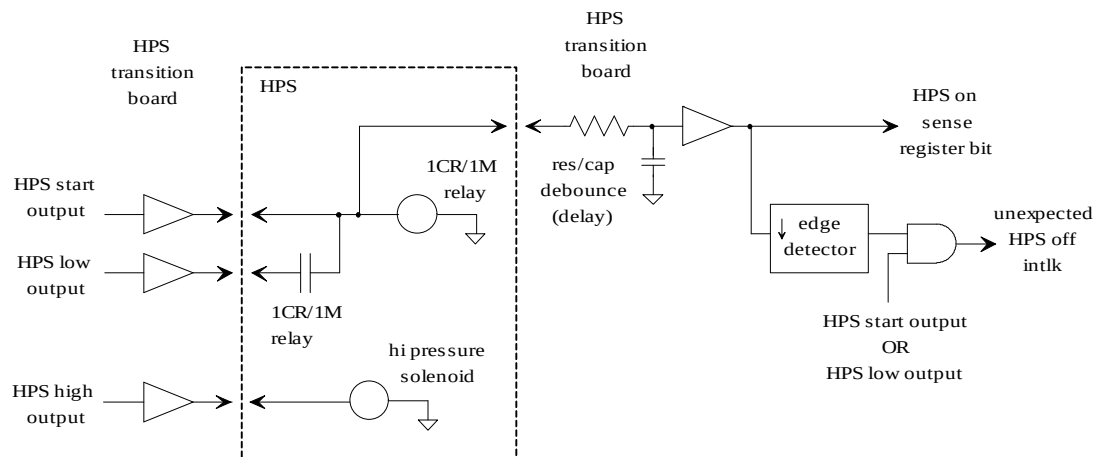
### starting the HPS

The HPS should be started only after the user presses the HPS low button on the pod or clicks the HPS low button on the software control panel. After an interlock, do NOT automatically clear the interlock and restart the HPS. The user must clear interlocks and then press the HPS low button again.

- Clear interlocks if necessary, see above.
- After any interlock the HYD ENABLE bits in the control register must be retwiddled. Do this by writing a 10b to the HYD ENABLE bits in the control register. Setting the HYD ENABLE bits must be done as a separate step from clearing the interlocks even though they are in the same register. This is due to timing considerations inside of the EPLD.
- Set the HPS START and LOW bits in the HPS register.

- After 5 seconds clear the HPS START bit leaving the LOW bit active. (Alternate – set the HPS START bit only, set the HPS LOW bit when the HPS ON SENSE line goes active (typically 50-100mS later).)
- Wait approx. 60mS and check the HPS ON SENSE bit in the HPS register, if it's 1 the HPS is latched on. If it's 0, the HPS is not on (due to an interlock, disconnected cable, etc.). If the HPS did not start, all bits in the HPS register must be cleared by software. Wait for the user to press the HPS low button again before attempting to start hydraulics again.
- To switch the HPS to high pressure, set the HPS HIGH bit (leaving the LOW bit set).
- To drop back to low pressure, clear the HPS HIGH bit.
- To switch the HPS off, clear all bits in the HPS register.

The sketch below shows a simplified partial schematic of an HPS and the HPS transition board. The sketch helps to show the details behind some of the interactions and nuances of the HPS interface. The details shown in the sketch are the same for any MTS HPS (except the 512 which doesn't have any remote start capabilities) and any MTS control panel (with or without the low current HPS interface). The only differences with the low current interface are the voltage and current levels.



### simplified HPS interface

#### observations on HPS interface

Note that because of the way that the HPS is connected, when the HPS START output is active, the HPS ON SENSE line will also be active. (Unless the HPS is disconnected or the HPS power is off. This is because the 3 HPS outputs on

the HPS board receive their power from the HPS – this isn't indicated on this drawing.)

The HPS ON SENSE bit will also show up as a 1 if the HPS is started from another controller in a multi-controller configuration.

Due to debouncing of the HPS ON SENSE signal, there will be a delay of up to 50mS before the change is visible in the HPS ON SENSE bit in the HPS register.

If the HPS switches to off *after it's started* (for reasons other than the HPS bits being cleared) it will generate an unexpected HPS off interlock. This will then clear the HPS bits.

#### historical perspective on HPS interface

Historically, older products such as the 458 keep the HPS START line active for as long as the user presses the HPS low button. The HPS LOW output goes active when the HPS ON SENSE signal becomes active tens of mS later (while the low button is still pressed). The HPS ON SENSE signal keeps the 458 and HPS latched on.

If the HPS doesn't start (due to an interlock, etc.), the HPS ON SENSE signal will not be active and the 458 will drop back to off when low is released. If the HPS ON SENSE signal goes inactive after the HPS has been latched on, it acts as an interlock and bumps the 458 to off.

#### HPS start signal duration

With a product like the 458 the HPS START output is active as long as the low button is pressed, which is typically hundreds of mS. Per the guys in the HPS group, this is more than long enough to start any MTS HPS that they are aware of.

There has been isolated, hard to document cases where certain HPS's need the HPS START output active for anywhere from 2 seconds up to 5 seconds. The design of the 458 allows the user to hold the low button for as long as necessary to latch the HPS on. When the duration of the HPS START output is fixed in either hardware or software it is probably necessary to design for the worse case and set the duration at roughly 5 seconds.

Pressing the HPS off button during the 5 second start period should drop the HPS back to off. Some older systems ignored the HPS off button during this time. This could be bad if the user notices the system doing something unexpected immediately after it's started.

This is the way that the HPS interface has operated for hundreds of years. If it's messy to implement the timing of the HPS START output in software with timers, etc. maybe it's worth considering tying the HPS START output to the pressing and releasing of the low button.

## interlock override

The HPS interlock override bit has been removed. This is at the recommendation of the HPS group who report that override should only be done when the user is standing at the HPS using the controls on the HPS.

## soft dump interlock

The soft dump interlock is a bit in the control register that can be set by software to dump the HPS and all stations (since it drives all of the station interlock lines active).

When clearing the SOFT DUMP bit, be aware of the following limitation of the hardware. Even though the SOFT DUMP bit is in the same register as the CLR INTLK bit and the HYD ENABLE bits, they can't be changed on the same write cycle to the control register. This is due to timing considerations inside of the EPLD (basically this is because all register bits are latched on the rising edge of the clock). When clearing a soft dump and starting hydraulics, there must be **3 separate writes** to the control register.

Clear the SOFT DUMP bit.

Set the CLR INTLK bit to clear the latched interlock.

Set the HYD ENABLE bits.

Start hydraulics as described above.

## support for all possible hydraulic configurations

There are non-obvious interactions between the HPS, HSM and crosshead unlock power output that tend to cause great pain and itch for the software folks.

There are 2 different types of interactions, interactions in the electronic hardware and interactions due to different combinations of hydraulic stuff.

The interactions on the electronics are due to:

- the crosshead unlock power output is the same signal as HSM high
- power for the proportional HSM circuit is switched thru the HSM low relay

This means that the HSM low and high relays need to be driven for most, if not all, hydraulic configurations.

Other than the 2 points listed above, there are no interactions lurking in the electronics. The HPS and HSM bits are really just dedicated digital I/O bits that drive relays or opto-isolators.

The interactions in the hydraulics are due to the different combinations of HPS, HSM and crosshead unlock power as listed in the table below. There are approx. 49,152.7 different possible configurations of the various hydraulic

components (HPS, HSM and crosshead unlock power). OK, that's a slight exaggeration, but it can be a mess.

Note that the 4 lines of the table aren't the only 4 possible combinations. Any of the 3 different HPS configurations in the table can be used with any of the 4 different HSM configurations which can be used with any of the 2 different crosshead configurations.

| hydraulic variables |              |           |
|---------------------|--------------|-----------|
| HPS                 | HSM          | CROSSHEAD |
| none                | none         | none      |
| on / off            | on / off     | on / off  |
| low / high          | low / high   |           |
|                     | proportional |           |

Yes, it's true that all systems must have a HPS, but not all systems have control of the HPS. Some larger labs have a centrally controlled house HPS with HSM's on each system.

On / off HPS's and HSM's use only the low bits for control (either the HPS LOW bit or the HSM LOW bit on the HSM transition board). The high bit is not used.

Observations and questions about the ramifications of this stuff:

The HSM low relay must be driven if the system is configured for a proportional HSM since the proportional HSM driver receives its power thru the HSM low relay contact. The low relay should be switched on at the start of the proportional HSM ramp up. The low relay should be switched off when the proportional HSM ramp hits zero when going to off. This will be handled by the proportional HSM circuitry on the HSM board.

The HSM high relay contact must be driven when there is high pressure to the load frame to allow the crosshead to be unlocked. This is true even if the system is configured for no HSM. This configuration has caused problems in the past, partially because systems without an HSM were frequently sold in the 1980's.

The electronics does allow the HSM to be switched on while the HPS is left off. This may or may not be valid, but the electronics doesn't care.

If a system doesn't have an HPS, will the user have to press HPS low and high buttons before being allowed to press HSM low and high?

If a system doesn't have an HSM, how will the crosshead unlock power output get twiddled?

Instron HSM's drop the low contact when they go to high pressure. Does this need to be supported? In the solenoid HSM mode, the hardware doesn't care and the low bit may be cleared when setting the high bit.

some solutions

For upgrades to older systems without an HSM the special versions of the 493.07 will be used. They have a crosshead unlock power output that is connected to the HPS high relay in the 493.07. These are part numbers 499694-05 (24V) and -06 (115V)

Instron and other vendor upgrades will be handled with the various versions of the 493.08 interface box, which were designed specifically for this task (OK, actually for use with the very similar 493.01 chassis).

## x.6 self test

---

None.

## x.7 diagnostics

---

Take it away, Roy.

# x.8 connections

J23      E stop out      D-9P

A form C relay contact is available on this connector. The relay will open if any E stop button connected to the chassis is hit.

J23 E stop output

| PIN | NAME   | FUNCTION                  |
|-----|--------|---------------------------|
| 1   | NC     | normally closed contact * |
| 2   | common | common                    |
| 3   | NO     | normally open contact *   |
| 4   | N/C    |                           |
| 5   | N/C    |                           |
| 6   | N/C    |                           |
| 7   | N/C    |                           |
| 8   | N/C    |                           |
| 9   | N/C    |                           |

\*Note that this relay is normally energized and drops out when an E stop occurs. This means that the normally closed contact is actually normally open and vice versa. The functions listed above reflect the labeling of the relay contacts, so when E stop is not active, pins 2-3 will be connected. When E stop is active, pins 1-2 will be connected.

J24 remote E stop in D-15S

This is electrically the same connector as J24 on the 493.01 chassis. It contains 2 circuits that are normally connected to a normally closed DPST E stop switch.

#### J24 remote E stop input

| PIN | NAME         | FUNCTION                                 |
|-----|--------------|------------------------------------------|
| 1   | N/C          |                                          |
| 2   | N/C          |                                          |
| 3   | N/C          |                                          |
| 4   | N/C          |                                          |
| 5   | local E stop | local E stop loop (connect to pin 7)     |
| 6   | N/C          |                                          |
| 7   | local E stop | local E stop loop (connect to pin 5)     |
| 8   | HPS E stop   | E stop loop from HPS (connect to pin 13) |
| 9   | N/C          |                                          |
| 10  | N/C          |                                          |
| 11  | N/C          |                                          |
| 12  | N/C          |                                          |
| 13  | HPS E stop   | E stop loop from HPS (connect to pin 8)  |
| 14  | N/C          |                                          |
| 15  | N/C          |                                          |

This is also electrically the same connector as on the 493.01 chassis. It uses the low level HPS interface. Depending on the flavor of HPS it will be connected either directly to the HPS or to the HPS thru a 493.07 HPS converter box. Refer to the *which pumps can it be connected to?* section of chapter 3 for more info.

#### J25 HPS connector

| PIN | NAME         | FUNCTION                                         |
|-----|--------------|--------------------------------------------------|
| 1   | HPS power    | 24 V from HPS                                    |
| 2   | HPS start    | H = HPS starting                                 |
| 3   | HPS low      | H = HPS low (or on)                              |
| 4   | HPS high     | H = HPS in high pressure                         |
| 5   | E stop       | E stop loop from HPS (24 V in)                   |
| 6   | E stop       | E stop loop from HPS (return)                    |
| 7   | 24 V out     | 24 V out (fused) for HPS defeat plug             |
| 8   | 24 V gnd     | ground for HPS defeat plug                       |
| 9   | HPS on sense | H = HPS on                                       |
| 10  | gnd          | ground from HPS (not connected to HPS board gnd) |
| 11  | over temp    | open = over temp interlock active                |
| 12  | low level    | open = low level interlock active                |
| 13  | N/C          |                                                  |
| 14  | N/C          |                                                  |
| 15  | N/C          |                                                  |

This was a spare connector with no designated function on the rear panel drawings that were circulated during concept development. The connector will NOT exist on the board.

This connector contains 3 digital inputs and 1 digital output. It didn't exist on the prototype boards.

#### J54 digital I/O

| PIN | NAME         | FUNCTION                                     |
|-----|--------------|----------------------------------------------|
| 1   | dig in 1 24V | 24V thru 15k resistor                        |
| 2   | dig in 1 hi  | hi side of opto-isolator (opto on = logic 1) |
| 3   | dig in 1 lo  | lo side of opto-coupler                      |
| 4   | dig in 1 com | 24V common                                   |
| 5   | dig in 2 24V | 24V thru 15k resistor                        |
| 6   | dig in 2 hi  | hi side of opto-isolator (opto on = logic 1) |
| 7   | dig in 2 lo  | lo side of opto-coupler                      |
| 8   | dig in 2 com | 24V common                                   |
| 9   | dig in 3 24V | 24V thru 15k resistor                        |
| 10  | dig in 3 hi  | hi side of opto-isolator (opto on = logic 1) |
| 11  | dig in 3 lo  | lo side of opto-coupler                      |
| 12  | dig in 3 com | 24V common                                   |
| 13  | spare        |                                              |
| 14  | dig out 1 hi | collector of opto-isolator                   |
| 15  | dig out 1 lo | emitter of opto-isolator                     |

internal connectors

J1 transition bus DIN-96P

Interface to the transition bus backplane.

J10 programming header 10 pin, 2 row Berg header

This is a header used to program the in circuit programmable Altera EPLD. It connects to an Altera BitBlaster which connects to the serial port of a PC (it can also be used with an Altera ByteBlaster which connects to the parallel port of a PC). Info on this header is in the BitBlaster and ByteBlaster sections of the Altera data book.

| J10 programming header |      |                            |
|------------------------|------|----------------------------|
| PIN                    | NAME | FUNCTION                   |
| 1                      | TCK  | clock signal               |
| 2                      | gnd  | ground                     |
| 3                      | TDO  | data from device           |
| 4                      | Vcc  | +5 V                       |
| 5                      | TMS  | JTAG state machine control |
| 6                      | N/C  |                            |
| 7                      | N/C  |                            |
| 8                      | N/C  |                            |
| 9                      | TDI  | data to device             |
| 10                     | gnd  | ground                     |

# x.9 configuration

---

There are no address select jumpers. A slot select line from the I/O Carrier board selects each board installed in the transition board backplane.

This board has no internal jumpers.

The following connectors require jumper plugs if no cable is installed in a system. They are the same jumper plugs as used on the 493.01 chassis. Check the drawings on DOD for the wiring of the jumper plugs.

|     |           |           |
|-----|-----------|-----------|
| J24 | E stop in | 397132-01 |
| J25 | HPS       | 397133-01 |

A jumper plug is not required for J54, digital I/O. If the digital inputs are left unconnected they will read back as 0.

## x.10 why did they do that?

---

Page 1

This section describes design details that aren't obvious to the casual observer (or something like that). This information could be useful for future modifications and fixes to the electronics. The information is organized by schematic page number.

Altera EPLD innards

The interface to the transition bus uses the same basic design as the other transition bus boards. Any non-obvious design details are listed in the TDF files.

The EPLD logic is written in Altera AHDL. The top level design file is HPS\_TRAN.TDF. Originally compiled with Altera MAX+ plus II version 9.21 running on a Win95 PC. The source files are stored on the Source Safe server.

Altera compile options: ?????????

List of Altera TDF files:

|           |                                                        |
|-----------|--------------------------------------------------------|
| HPS_TRAN  | top level design file, contains all inputs and outputs |
| LOC_DTACK | DTACK state machine                                    |
| MUX81     | 8 to 1 mux for reading register data bits              |
| DEBOUNC_R | debounce function, mimics Motorola MC14490 debounce IC |

The fail, pwr\_fail and station intlks have debouncing inside the EPLD. This was added in the rev. B PWB layout. The original design didn't debounce these 3 signals from the backplane, but ESD testing demonstrated the need. Since the EPLD was being changed to a larger part, the extra resources need for debouncing weren't a problem. This was easier than adding hardware debounce circuits.

Pull-up resistors are used on the HPS start, low and high lines to ensure valid logic high levels and to pull the lines inactive if the EPLD is blank or the outputs are hi-Z for some reason.

Page 2

This page implements the low level HPS interface. It's the same HPS circuitry as used on 493.01 Europa board, except the opto-isolators have been changed to match the parts used on the digital I/O.

The E-stop chain from the backplane is used to drive the coil of a relay. This isolates the backplane from the E stop lines from the HPS. It also allows monitoring of the state of the E stop relay and provides a set of contacts used for E stop out.

The CE requirements for E stop state that only hardwired electro-mechanical components can be used for E stop circuits.

The digital I/O circuits are very similar to those used on 493.01 Europa, except the opto-isolators have been changed to higher gain parts. The higher gain is needed to allow lower input currents over a wide input voltage range. This allows the inputs to accept up to 26V (an improvement over Europa) and not need a 25W resistor in series with the opto input.

#### PWB and manufacturing info

The PWB is 0.062" thick FR-4 fiberglass. It has 4 layers: 2 power and ground layers and 2 signal layers.

The trace / land widths are 8/8 mils. The copper thickness is 2 oz. on outside layers and 1 oz. on inside layers.

The design is mixed SMD and thru-hole. All components are mounted on the primary side of the PWB.

The smallest lead pitch is 0.020" on the Altera EPM7128 EPLD, which is in a 100 pin TQFP package.

## x.11 timing diagrams

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None.

## x.12 list of related drawings

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### drawing part numbers

| PART NUMBER | DESCRIPTION                                  |
|-------------|----------------------------------------------|
| 100-003-855 | top level assembly                           |
| 700-000-043 | PWB schematic                                |
| 100-001-994 | PWB                                          |
| 100-001-997 | circuit board assembly                       |
| 700-000-694 | Altera EPLD programming instructions drawing |
| 100-000-656 | Cobra MC cable selector drawing              |
| 100-000-654 | Cobra MC setup / config drawing              |