

493.74 HSM transition board

This functional specification covers the 493.74 HSM transition board for the multi-channel / multi-station Cobra VME product.

Greg Ness Feb-3-00 revision 0.9

Contents

x.1 introduction	3
x.2 specifications	6
x.3 functional description	8
x.4 registers / address map	16
x.5 processor code	35
x.6 self test	41
x.7 diagnostics	41
x.8 connections	42
x.9 configuration	46
x.10 why did they do that?	48
x.11 timing diagrams	51
x.12 list of related drawings	51

change log

Feb-3-00	rev. 0.9	added step to 0 bit to control register added clear intlk 2 bit to control register added station interlock bit to intlk register added change bars for changes since rev. 0.4A
Oct-25-99	rev. 0.5	misc tweaks after proto checkout changed 24V fail intlk to power fail updates to intlk drawing, see text before drawing clarified prop HSM state graph changed font for better readability added table of contents
Apr-28-99	rev. 0.4A	re-arranged pin outs on J44 and J49 added illegal proportional HSM value intlk bit many clarifications on register bit interactions added opto-isolator intlk output to J44 listed intlks that drive station line vs. HSM dump added register cheat sheet to register section added text to <i>Why did they do that</i> section
Feb-9-99	rev. 0.3A	tweaks to registers and processor code sections rearranged some bits to match HPS board
Dec-9-98	rev. 0.2A	minor revisions after design review
Nov-25-98	rev. 0.01A	initial document

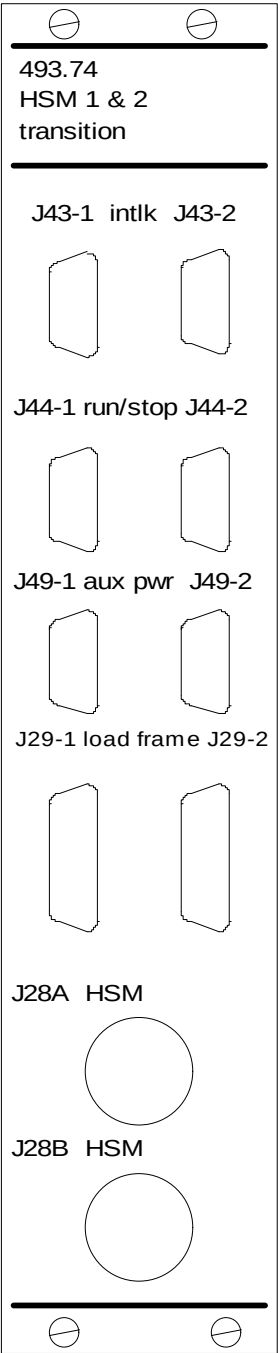
x.1 introduction

The 493.74 HSM transition board plugs into the rear panel of the multi-channel Cobra VME chassis and can accommodate up to 2 channels and 2 stations (typically). It is a double wide module that provides the following features:

- 2 HSM connectors that may be configured to drive:
 - 24Vdc off/lo/hi (or on/off) solenoids, OR
 - 24Vdc proportional solenoids
- 2 load frame connectors that each contain:
 - E stop / station stop input
 - crosshead unlock power output
 - crosshead unlock event input (usually used for program interlock)
- 2 general purpose interlock connectors, each with:
 - interlock input to shut down hydraulics at the assigned station
 - event input to generate a user definable action (selected in software)
- 2 sets of run/stop connectors that each contain:
 - 2 form C run/stop relay contacts on each connector
 - interlock status outputs (opto-isolators)
- 2 poly fused aux power outputs, each containing:
 - ± 15 Vdc
 - 24 Vdc
 - 5 Vdc

front panel view

Below is a rough artist's conception of the front panel of the HSM transition board. Not to scale.



internal features

no processor

no RAM

no serial EEPROM

no watchdog timers

no DC fail detectors

This board is designed to plug into the transition bus which is driven from the VME I/O Carrier board. It will appear in the VME address space of the Carrier. The interface to the Carrier is a simplified VME style interface configured as A10:D16 and a minimal number of control lines.

A slot select line from the Carrier will enable each transition board as required. This results in no address jumpers to set incorrectly.



Warning : The next paragraph discusses the maximum number of stations that are supported by the *hardware*. This is **NOT** the same as the number of stations supported by the *software*. The currently planned software supports up to 4 stations.



The resources of this board can be assigned, thru software, to any of 8 stations*. Each station has its own interlock line on the backplane to allow multiple boards to operate together as a single station. A station interlock will drive the appropriate station interlock line active on the backplane, which will dump all HSM's assigned to that station.

The 24V fail detector has been removed from the board. It has been replaced by the DC fail detectors on the power distribution board.

*Note that the current software will allow the use of up to 4 stations per chassis.

x.2 specifications

493.74 HSM transition board specifications

	PARAMETER	SPECIFICATION
general	power requirements	includes HSM board only, does NOT include external loads (HSM and aux power outputs)
	+5 Vdc	
	±12Vdc	
	±15 Vdc	250 mA
	+24 Vdc	none 15 mA 75 mA
	typical HSM loads: 6 x 0.75 A per 24V sol.	4.5 A
	power dissipation, solenoid mode	4W max
	power dissipation, proportional mode	11W typical, 19W max
	operating temperature range	5-40°C
	humidity	0-85%, non condensing
	altitude	10,000 ft max
	PWB size	233mm x 80mm (9.2" x 3.1")
E stop input	max voltage / current	24 Vdc, 50 mA max
HSM, solenoid	max current	1.0 A* at 24 Vdc
	max number of solenoids	6 (2 each of low, high and crosshead unlock)
HSM, proportional	nominal full scale current	0.7 A
	min high output voltage	20 Vdc (TBD)
	min valve resistance	20Ω
	ramp time (0 to full scale)	2.1 or 4.2 S (selectable w/register bit)
run /stop relay	max voltage / current	1 A at 30 Vdc/ac
inputs (J43 intlk, J43 event and J29 xhead intlk)	V _{IH} min on voltage	3.0 V at 0.3 mA

	V _{IL} max off voltage	0.8 V
	max voltage	26 Vdc at 3.8 mA
	input resistance	6.6 kΩ
load frame	crosshead unlock output	1.0 A* at 24 Vdc
	crosshead unlock interlock	refer to interlock input, above
	E stop input	refer to E stop spec, above
aux power output	max output current +5 V ±15 V +24 V	0.75 A (at max temperature) 0.75 A (at max temperature) 0.75 A* (at max temperature)
interlock status opto-isolator outputs (J44)	output format	open collector, open emitter transistor
	max voltage	26 Vdc
	min guaranteed output current drive	20 mA (30 mA typical) at 1.0 V max
	max output current without damage	80 mA
	max output power dissipation	110 mW

*max current from 24 V supply can not exceed 4.8A for all loads driven from HSM board:

- HSM's
- crosshead unlock solenoid power
- aux power output

24V source on HSM board has an internal 5.0A poly fuse (5.0A at max temperature).

x.3 functional description

HSM

This board can be used with either 24V off/lo/hi or 24V proportional HSM's. The proportional HSM driver circuit is built in. The chassis internal 24V power supply provides the power for either flavor of HSM.

This board is not directly usable with 115V HSM's. Applications that require 115V HSM's will have to use an external converter box (413.08).

The type of HSM, either off/lo/hi or proportional is selected via software by twiddling a register bit.

The HSM connector is the familiar 4 pin CPC that we all know and love. The cable is the same as the one used on the 493.01.

The chassis contains a 24V supply for powering 24V HSM's. The table below lists some different combinations of HSM loads that are possible **based ONLY on the size of the 24V power supply in the 10 slot VME chassis**. Note that the current software supports up to 4 stations. Assumptions used to create the table:

- The use of the typical 0.75A HSM solenoid.
- 2 (or 3) HSM boards are used in a chassis with a 10A HSM power supply.



WARNING: The currently planned software supports up to 4 stations.



HSM/xhead	number of each HSM/xhead			
lo/hi	4	4	6	0
on/off or prop	0	0	0	6
crosshead	4	0	0	6
# of solenoids	12	8	12	12
amps	9	6	9	9
watts (at 24V)	216	144	216	216

load frame

These functions are provided on the J29 Load Frame connector:

- E stop / station stop input
- crosshead unlock power output
- crosshead unlock event input (usually used for program interlock)

The E stop input is actually 2 separate inputs, similar to other products. The 1st set of inputs generates a local interlock to shut down the assigned station. Assigning stations is discussed in the interlock mapping section, ahead. The 2nd input goes directly back to the HPS and generates a redundant shut down of the pump.

The E stop input may be used as either an E stop input or a station stop input. To use it as E stop, both circuits must be connected to the E stop switch. To use the input as a station stop, only the local interlock circuit is wired to the switch. A station stop will shut down only the HSM's associated with that station and the HPS will continue to run for other stations.

The voltage on the E stop switch output is always 24Vdc at a low current (50mA max). This means that a chassis ground in the E stop cable is not required.

The crosshead unlock power is from the HSM high contact. It will always be 24Vdc. This output allows the crosshead of some load frames to be unlocked only when the HSM is in high pressure. Refer to the μ P code section of this spec for information on handling the zillions of variations of hydraulic configuration (mixing different combinations of HSM types and HPS types).

The crosshead unlock interlock (event) input typically goes to a normally closed switch on the load frame that indicates the status of the crosshead unlock solenoid. Unlocking the solenoid opens the switch contacts. This sets a bit in the event register and software determines what to do with the bit. The historic use is to prevent the user from starting the program while the crosshead is unlocked.

This connector is electrically the same as on the 493.01. However, due to space constraints on the rear panel, the connector type had to be changed from the familiar CPC-14S connector to a 15 pin D connector.

general purpose interlock input

The interlock connector has 2 separate inputs, 1 to generate a station interlock and an event that is just a register bit that is passed on to software for a user selectable action.

The inputs may be used with either mechanical switch contacts or logic outputs. The input is debounced in hardware. This connector is the same as on 493.01, except in a 9 pin D instead of a 15 pin D.

aux power output

5V, ± 15 V and 24V are provided straight from the Cobra internal power supply for driving external high level conditioners, proximity switches, solenoids, flashing LED's, sirens, defibrillators, Jacob's ladder transformers or whatever else you want. Note that these outputs are power supply outputs and not reference voltages, there will be some drift and variation from the nominal voltage due to power supply component tolerances and changes in the loading and temperature. The stability and accuracy of these outputs are determined by

the specs for the Cobra internal power supply. Consult the power supply spec. for details.

Caution

All outputs are fused internally at 0.75A (worst case at max temperature) to protect Cobra, the servo loop and the system cable in case of an external short. Since the fuses do not open instantaneously in response to an overload, they will not provide bulletproof protection against all types of overloads. The fuses are of the self-resetting type. In the event of an overload, turn the power off, wait approx. 1-2 minutes and try again.

If that doesn't work, try this: turn the power off, **remove the short this time**, wait approx. 1-2 minutes and try again. Is that better?

run/stop relay contacts

Each of the 2 run/stop connectors has a separate relay for indicating the run/stop status of the system. Each relay has 2 form C contacts (DPDT) available on the D connector. These relays are under software control and are not affected by any interlocks.

As added features on the run/stop connector, at no additional cost, are opto-isolators for indicating the state of interlocks on channel A or channel B. These outputs are normally on and will turn off in the event of an interlock. These are provided for indicating interlock status to external devices.

A jumper is provided to change the outputs from indicating the state of the interlock inputs for a given channel OR indicating the state of the interlocks as seen by the HSM on that channel. Refer to the interlock drawing on the next page for details. The jumper selects whether the interlock output is connected to the OR gate on the left that drives the station interlock line or to the OR gate on the right that drives the dump HSM signal.

interlock mapping

The interlock sources (from the load frame and interlock connectors) on each channel of the HSM board can be mapped to any 1 of the 8 station interlock lines* on the backplane. Each of the 2 HSM outputs can similarly be mapped to any 1 of the 8 station interlock lines.

WARNING: *The currently planned software supports up to 4 (four) stations.

Each interlock source and each HSM must be assigned to a station interlock line. The interlock sources on each board are assigned into 2 groups, each of which can be assigned separately. Along with the 2 HSM's this results in 4 separate mappings that must happen on each board.

An interlock will drive the assigned station interlock line active on the backplane, which will dump the HSM's assigned to that station, including those on other HSM boards.

If the resources of a board aren't mapped, an interlock will be generated and the HSM's will not be allowed to be switched on.

The drawing on the next page shows the interlock functionality of the HSM and HPS transition boards along with the transition backplane.

The interlock drawing was updated on Oct-21-99 and then again on Dec-8-99 with these changes, most of which have been in place for a while:

- ◆ added power fail line on backplane (was always in hardware)
- ◆ deleted 24V fail detector on HSM board, now tied to power fail on backplane
- ◆ added station intlk monitoring (SW controlled) to HPS board, part of change request approved Sep-20-99
- ◆ listed hydraulic enable intlk on both boards (was always in the hardware)
- ◆ listed illegal proportional HSM values intlk on HSM board (was always in hardware)
- ◆ added 3rd OR gate for interlocks and did rearranging of interlocks to keep interlocks associated with the HSM from the interlock OR gate (OR1) to one of the HSM OR gates (OR2 and OR3)

multi-station Cobra interlocks

transition boards

transition board
backplane

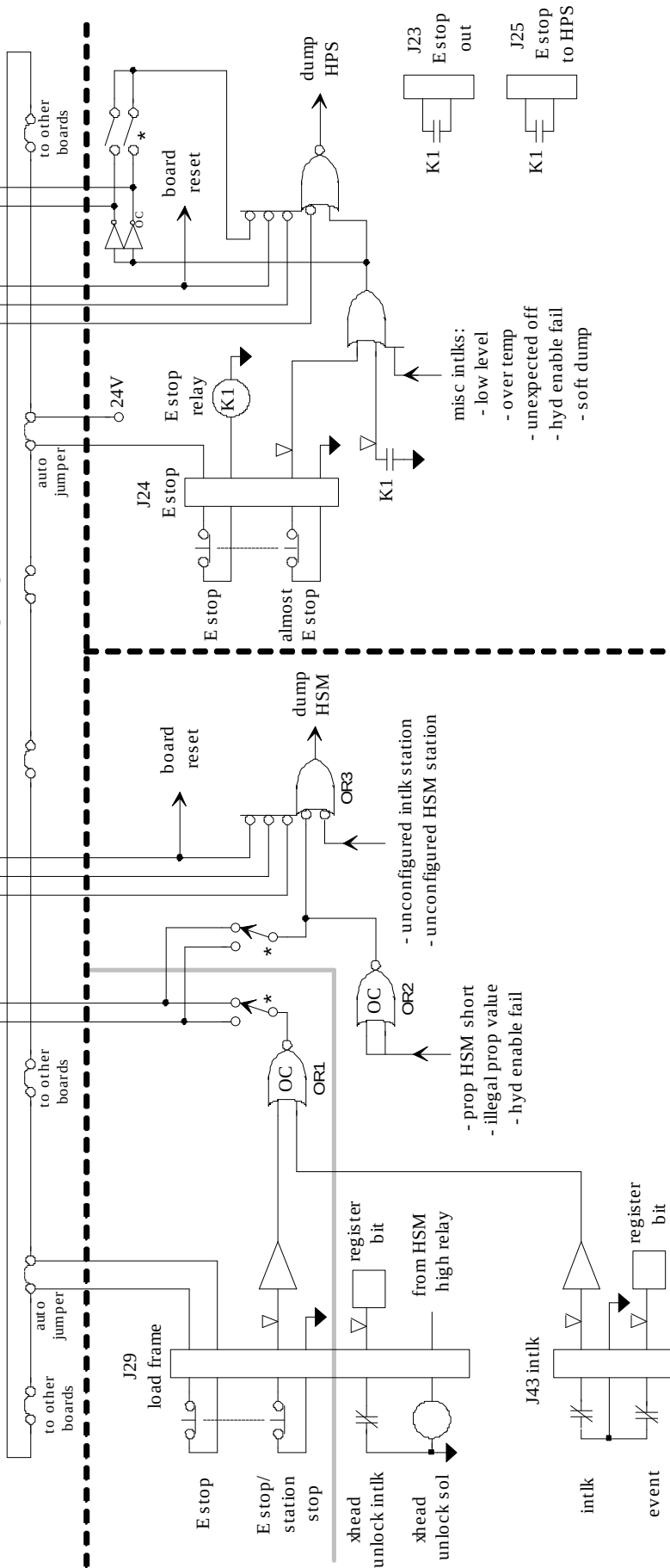
/station interlock lines,
2 of 8 lines shown

/reset (from Carrier)

/fail (from Carrier)

/power fail (from power supply)

E stop loop



HSM transition board
(1 of 2 stations shown)

GRES pod transition board uses E stop
circuitry enclosed by shaded lines

all interlocks are individually latched
and have separate register bits for readback

* hardware assignments
controlled by register bits

max number of HSM boards in a system

There are no *hardware* limitations on the number of HSM boards in a system EXCEPT for the power supply current on the internal 24V supply. The worst case current draw on 24V (external HSM and crosshead solenoids and aux power loads) must not exceed the amount of 24V available (refer to the chassis/power supply spec and the table near the start of this functional description section). The worst case 24V current also must not exceed any of the specs for the HSM board, see section 2, above. There may be 0, 1 or more HSM boards in a system. Note that the software folks may have a different opinion on this topic.

WARNING: The currently planned software supports up to 4 stations.

A typical 4 channel/station system would have 2 HSM boards and 1 HPS board. The power supply in the 10 slot chassis will drive this configuration, no problem (with typical HSM loads (0.75A per solenoid)).

An HPS transition board is required to allow proper operation of the E stop circuitry.

Note that the transition board backplane has 8 station lines and a single E stop loop that is used for all transition boards.

labeling of connectors

Note that the labeling of the connectors was changed several months before the product was released. The original prototypes had all connectors labeled with either an –A or –B suffix to indicate the associated channel. Each of the 2 channels can then be mapped, via software, to any of 8 stations. Letters were used to avoid indicating any association with channel numbers and to be consistent with other products.

For somewhat unclear reasons, it was decreed that using the same suffix for both the interlock inputs and the HSM outputs was confusing because they could be mapped separately. The interlock connectors now have either a –1 or a –2 suffix to indicate they are somewhat fixed in their station assignment. The HSM connectors retained the –A or –B suffix.

For reasons that are even less clear, no one is concerned about trying to indicate mapping of the connectors/resources on other boards in the system – despite having the same problem of unclear station assignments.

In the rush to update front panel graphics, schematic and PWB reference designators, functional spec references, etc. to indicate the new suffixes, it's possible that some references to the older letter suffixes were missed. Oops.

internal stuff

The HSM board is controlled by registers that are accessed on the VME bus thru the Carrier board. Multiple slot select lines from the Carrier eliminates the need for address switches on any transition board.

The HSM board is connected to the VME Carrier board thru the A10:D16 transition board bus (patent pending).

proportional HSM circuitry

The proportional HSM circuitry in the EPLD (electrically programmed logic device) generates the ramp needed to cycle the proportional HSM on or off. Software twiddles bits in the registers to specify the low pressure setting and the hardware does the rest (OK, this is a slight oversimplification). Status bits are provided to allow the software to determine if the proportional HSM is at an endpoint (fully off, low or high) or currently ramping between endpoints.

To simplify the proportional ramp circuitry, only 2 different rates will be available. The low and high pressure settings will be adjustable. Once a rate is selected the time between any 2 endpoints will change if the low or high pressure setting is changed. The software should take this into account when allowing the user to specify levels or turn on/turn off times.

The proportional HSM ramps between all endpoints (off, low or high) at the specified rate. The only exception is if an interlock occurs, in which case it steps immediately to 0.

The proportional HSM DAC is an 8 bit DAC, same as on existing 490.60 and 493.01 products.

programmable logic

The logic for the operation of the board is contained in an Altera 10K series EPLD. This part is programmed with a one time programmable serial configuration PROM in a socketed 8 pin DIP package.

analog supply voltage

This board uses $\pm 15V$. In theory, it could run on $\pm 12V$ if $\pm 15V$ is not available. This could be necessary if the $\pm 15V$ supplies are eliminated someday, which has been discussed repeatedly during the development cycle.

Tests will be done on the prototypes to verify that everything works OK on $\pm 12V$. In theory, the only difference visible from the outside is that the $\pm 15V$ outputs on the J49 aux power connectors will be $\pm 12V$.

The prototypes will have jumpers to select between $\pm 15V$ and $\pm 12V$ for all on-board sources (including the aux power outputs). These jumpers may or may not be present on the production boards.

$\pm 15\text{V}$ is used for:

proportional HSM circuit:

DAC

HSM short detector comparator

5V reference, used by:

proportional HSM DAC

J49 aux power output connector

x.4 registers / address map

software identification of transition boards

Each slot select line on the transition board backplane will have a weak pull down on the Carrier (or the transition board backplane). Each transition board will have a strong pull up on the slot select line. A register on the Carrier will allow the state of these lines to be read back. A 0 will indicate an open slot and a 1 will indicate an installed transition board.

Alternatively, an attempt could be made to talk to each transition board slot. The lack of a response from any empty slot will generate a BEER.

Each board will have a board ID register at the first address location. This will allow the software to determine the type of board in each slot.

registers and address map

There are no address select jumpers on the transition boards. Their address is determined by the slot position in the backplane. A separate slot select line from the I/O Carrier board is routed to each slot.

Below is a table of the registers on the HSM transition board. The addresses listed must be added to the offset due to the slot address (dependant on the transition bus slot) and also to the base address on the I/O carrier board.

Only 6 out of 10 address bits are decoded on this board. This means that images of these registers will appear at addresses that are multiples of 0x80. Other addresses might NOT return a DTACK and will generate a bus error (TBD).

The architecture of the transition bus supports only D16 transfers.

Below is an equation that details how to determine the VME address of a particular transition board register given the I/O Carrier base address, the transition bus slot number and the transition board address (from the table in the next section). Even though the transition bus uses 10 address lines, the transition board addresses are on 0x10000 boundaries to match the 493.01 chassis.

$$\text{VME_address} = \text{Carrier_base} + (0x10000 * \text{slot_number}) + \text{reg_address}$$

Accesses to addresses not listed in the table below will NOT generate a DTACK and will be terminated with a bus error.

All of the registers, except for the board ID register, are in 2 identical sets with the 1st set for channel A and the 2nd set for channel B. Since they are the same, they are only described once in the text below.

All addresses are in hex.

At the end of this section is a 1 page cheat sheet of register address and bits for quick reference.

address map

register address map

REGISTER	ADDRESS	READ/ WRITE	WIDTH (BITS)	INITIAL VALUE
board ID	00	R	16	0x0051
ch. A, intlk to station mapping	20	R/W	16	0
ch. A, HSM to station mapping	22	R/W	16	0
ch. A, interlock	24	R	16	*
ch. A, event / HSM status	26	R	16	0
ch. A, control	28	R/W	16	0
ch. A, HSM	2A	R/W	16	0
ch. A, prop HSM low value	2C	R/W	16	0
ch. A, prop HSM high value	2E	R/W	16	0
ch. B, intlk to station mapping	40	R/W	16	0
ch. B, HSM to station mapping	42	R/W	16	0
ch. B, interlock	44	R	16	*
ch. B, event / HSM status	46	R	16	0
ch. B, control	48	R/W	16	0
ch. B, HSM	4A	R/W	16	0
ch. B, prop HSM low value	4C	R/W	16	0
ch. B, prop HSM high value	4E	R/W	16	0

*The interlock register will power up with the current latched state of the interlocks. Either that or just garbage. Or maybe some combination of the 2, we just don't know (this is the same as the existing 493.01 motherboard).

This section contains information on the individual register bits with a short description of each bit. Details on the interactions between different bits and specific procedures (clearing interlocks, etc.) are described in the next section (processor code).

Unused register bits read back as 0. They may be written with any value.

board ID register

This read only register reads back a unique ID number to let the software determine what is installed in each transition board slot.

board ID register (addr 00)		
BIT	NAME	FUNCTION
0-15	board ID	0x0051

TBD – the upper byte of the board ID may be used to indicate a change to the functionality of the board as seen by the software.

interlock mapping registers

The channel A/B interlock station mapping registers controls which of the 8 station interlock lines the channel A/B interlock sources (J29A station stop and J43A interlock) are tied to on the transition bus backplane. The channel A interlock sources are OR'ed together and are mapped as a single unit with the channel A register (at address 20). See the interlock diagram in the interlock mapping section of the functional description for a pictorial view of how this works.

Similarly, the channel B interlock sources (J29B and J43B) are OR'ed together and are mapped as a single unit with the channel B register (at address 40).

WARNING: The currently planned software supports up to 4 stations.

If an interlock source is not mapped to a station, an unconfigured station interlock will be generated that will prevent the HSMs from starting.

The intent is that the interlock sources are tied to a single station interlock line, but the hardware does not prevent them from being mapped to multiple interlock lines. This means that more than 1 bit can be set in this register to drive more than 1 station interlock line active when an interlock occurs.

channel A/B interlock station mapping register (addr 20, 40)

BIT	NAME	FUNCTION
0	station 1	0 = not mapped to station 1 1 = interlocks mapped to station 1
1	station 2	0 = not mapped to station 2 1 = interlocks mapped to station 2
2	station 3	0 = not mapped to station 3 1 = interlocks mapped to station 3
3	station 4	0 = not mapped to station 4 1 = interlocks mapped to station 4
4	station 5	0 = not mapped to station 5 1 = interlocks mapped to station 5
5	station 6	0 = not mapped to station 6 1 = interlocks mapped to station 6
6	station 7	0 = not mapped to station 7 1 = interlocks mapped to station 7
7	station 8	0 = not mapped to station 8 1 = interlocks mapped to station 8
8-15	unused	reads back as 0

HSM station mapping registers

The channel A/B HSM station mapping registers control which of the 8 station interlock lines on the backplane are mapped to each of the 2 HSM's. An interlock on the station line that is mapped to a given HSM will shut down that HSM. Each of the 2 HSM's can be mapped to a separate station using the 2 separate registers.

WARNING: The currently planned software supports up to 4 stations.

If a HSM is not mapped to a station, an unconfigured station interlock will be generated and the HSM will be prevented from starting.

The intent is that an HSM will be tied to a single station interlock line, but the hardware does not prevent an HSM from being mapped to multiple interlock lines. This means that more than 1 bit can be set in this register to dump the HSM if any of the selected station interlock lines go active.

channel A/B HSM station mapping register (addr 22, 42)

BIT	NAME	FUNCTION
0	station 1	0 = not mapped to station 1 1 = HSM mapped to station 1
1	station 2	0 = not mapped to station 2 1 = HSM mapped to station 2
2	station 3	0 = not mapped to station 3 1 = HSM mapped to station 3
3	station 4	0 = not mapped to station 4 1 = HSM mapped to station 4
4	station 5	0 = not mapped to station 5 1 = HSM mapped to station 5
5	station 6	0 = not mapped to station 6 1 = HSM mapped to station 6
6	station 7	0 = not mapped to station 7 1 = HSM mapped to station 7
7	station 8	0 = not mapped to station 8 1 = HSM mapped to station 8
8-15	unused	reads back as 0

interlock registers

All of the interlock sources on the HSM board have a separate bit in one of the 2 read only interlock registers. They are separated into channel A interlocks and channel B interlocks. Interlocks that are common to both channels (backplane fail line, reset/power up and power fail) appear in both registers.

All of the interlocks are individually latched and are cleared with the clear interlock bits in the control register. An active interlock has priority over the clear interlock bit.

There is no lockout of interlocks in hardware, the software must keep track of the first interlock to go active. This allows the user to determine which interlock initiated the shut down when multiple interlocks become active during the shutdown. This is not a problem for the SW guys.

Note that about half of the interlocks on this board drive the backplane station interlock line (as selected with the interlock OR HSM mapping registers). The other half of the interlocks dump the HSM directly, regardless of its station mapping. This is shown by the 3 OR gates in the interlock diagram. Part of the idea is that interlocks that are already visible on the backplane (fail, power fail and reset) shouldn't drive the station interlock lines since all boards can already see the original interlock. The table below lists the category for each interlock along with the register bit number.

drives station line selected by interlock mapping register (OR1)

J43 interlock (8)
J29 station/E stop (10)

drives station interlock line selected by HSM mapping register (OR2)

hyd enable fail (6)
prop HSM short (12)
illegal prop HSM value (13)

dumps HSM directly without driving any station interlock lines (OR3)

power fail (0)
unconfigured HSM (2)
unconfigured intlk source (3)
fail line from backplane (4)
selected station intlk line (14)
reset line from backplane (15)

The state of the individual station interlock lines on the transition board backplane can be monitored from a register on the Carrier board. The Carrier board also allows driving any station interlock line active.

As of Jan-00 (proto PROM rev. 5 and up) station interlock is now a debounced, latched register bit. All interlock sources that can dump hydraulics now have a latched bit in the interlock register. This was added after ESD testing showed that momentary transients could dump the HSM by tripping the station interlock lines, but not leave any trace of what happened.

To fix this problem, a debounce circuit was added inside of the EPLD for the station interlock, fail and power fail lines. Further testing showed that this prevents dumps due to ESD. Adding the latched register bit for station

interlock provides the trail of bread crumbs if this sort of goofy stuff happens again.

The fail, power fail and station interlock lines are debounced in the EPLD. The proportional HSM short, J43 intlk, J29 station stop interlocks (along with J43 event and xhead event) are all debounced in external hardware (RC networks with HC14's).

Important note about reporting interlocks

It is important that the software report a unique, descriptive error message for EACH active interlock – similar to the 493 system. This is a must for troubleshooting systems, both in house and in the field. Some older systems lumped many interlocks into a few categories and reported a vague error message (i.e. controller interlock) which greatly hindered troubleshooting because much time is wasted trying to determine exactly which interlock is active.

It's true that the names of some of the obscure internal interlocks won't mean much to a customer or FSE, however, if/when they contact headquarters for additional assistance in solving a difficult problem, the description of the exact interlock that has been tripping will be invaluable.

With the HSM board it's important to also list the board slot number and/or channel number because there are 2 channels on each HSM board and typically 2 or more HSM boards per system.

interlock A/B registers (addr 24, 44)

BIT	NAME	FUNCTION
0	power fail	0 = no interlock 1 = power fail line active on backplane
1	unused	reads back as 0
2	unconfig HSM	0 = no interlock 1 = unconfigured HSM station map register, intlk active
3	unconfig intlk source	0 = no interlock 1 = unconfigured intlk source station map register, intlk active
4	fail line intlk	0 = no interlock 1 = fail line active on backplane
5	unused	reads back as 0
6	hyd enable fail	0 = no interlock 1 = incorrect hyd enable sequence used
7	unused	reads back as 0
8	J43 interlock	0 = no interlock 1 = interlock from J43 interlock connector
9	unused	reads back as 0
10	J29 station stop / E stop	0 = no interlock 1 = interlock from J29 load frame connector
11	unused	reads back as 0
12	prop HSM short	0 = no interlock 1 = proportional HSM short interlock
13	illegal prop HSM value	0 = no interlock 1 = illegal settings for prop HSM stuff
14	station intlk	0 = no interlock 1 = station interlock line active on backplane
15	reset /power up	0 = no interlock 1 = reset / power up interlock active

(0) The power fail line is active if the power fail line on the backplane is active. This is driven by the DC fail detectors on the power distribution board. It monitors all power supply outputs. (Formerly 24V fail, changed Sep-99.)

(2) The unconfigured HSM interlock is active if the HSM hasn't been assigned to a station with the HSM station mapping register (the HSM mapping register must be non-zero). See the processor code section for information on handling unused channels.

(3) The unconfigured interlock source interlock is active if the interlock source hasn't been assigned to a station with the interlock station mapping register (the interlock mapping register must be non-zero). See the processor code section for information on handling unused channels.

(4) The fail interlock is active if the fail line on the backplane is driven active by the Carrier board.

(6) The hydraulic enable fail interlock is active if the hyd enable bits in the control register aren't set to the correct state before writing to the hydraulic register. This is a safeguard against random writes from starting hydraulics.

(8) The J43 interlock is active if the switch contact on J43 is open.

(10) The station stop interlock is active if the E stop / station stop switch contact on J29 is open. Both E stop and station stop appear the same as viewed from this board (both will set this bit). An E stop will also set the E stop interlock bit in the interlock register on the HPS board.

(12) The proportional HSM short bit is active if the load on the proportional HSM output is less than approx. 18Ω . This interlock is provided to prevent excessive power dissipation in the proportional HSM transistor if the load is shorted or the cable is wired backwards (a reversed cable will make the solenoid appear like a short due to the snubber diode). This interlock is enabled only when the HSM mode bit (control register, bit 12) is set for proportional HSM. (Added Apr-1-99.)

(13) Illegal proportional HSM value is generated by any of the following conditions:

- the value in the HSM low register is 0, or
- the value in the high register is less than or equal to the value in the low register, or
- HSM high bit is set AND HSM low bit is cleared.

This interlock is required to prevent the hardware from doing bad things if the low or high value registers are loaded incorrectly. This interlock is enabled only when the HSM mode bit (control register, bit 12) is set for proportional HSM. (Added Apr-1-99.)

(14) The station interlock bit is set if the station interlock line that the HSM is mapped to becomes active.

(15) This bit is the reset / power up interlock. It will be set at power up or when the reset line on the backplane is active. This interlock was added in Jan-99 to allow visibility for the case where the reset line on the backplane goes active and causes the hydraulics to shut down. Without this bit, the hydraulics would just appear to go inactive with no trace of what made it happen.

event / proportional HSM status registers

The proportional HSM status bits are combined with the event bits into these registers to minimize the number of registers that must be regularly polled by the software. These registers are read only.

event bits

All of the event sources on the HSM board have a separate bit in one of the 2 event/ proportional HSM status registers. They are separated into separate registers for channel A and channel B.

All of the events are individually latched and are cleared with the clear interlock 2 bit in the control register. An active event has priority over the clear interlock 2 bit.

There is no lockout of events in hardware, the software must keep track of the first interlock/event to go active.

No action is taken by the hardware if the events are active. They will typically perform a user definable action that can be set up in the software.

proportional HSM status bits

The status bits allow software to monitor the state of the proportional HSM circuitry (in low, ramping to high, etc.). The HSM status bits are not affected by the clear interlock bit and will update in real time as the proportional HSM status changes.

The status bits indicate the state of the HSM in both modes, solenoid or proportional. When in solenoid mode, the ramping bits aren't used. (The software guys want the HSM status bits to function in both HSM modes.)

The bits indicate the correct HSM status in solenoid mode. Here is the logic used to generate the HSM status bits in the solenoid mode. The HSM command bits are the bits in the HSM register.

status	HSM command bits
off	low NOR hi
low	low AND NOT hi
high	hi

event / proportional HSM status A/B registers (addr 26, 46)

BIT	NAME	FUNCTION
0	HSM off	0 = HSM not off 1 = HSM off
1	HSM low	0 = HSM not in low pressure 1 = HSM in low pressure
2	HSM high	0 = HSM not in high pressure 1 = HSM in high pressure
3	unused	reads back as 0
4	HSM up to low	0 = HSM output is not ramping up to low 1 = HSM output is ramping up to low pressure
5	HSM up to hi	0 = HSM output is not ramping up to high 1 = HSM output is ramping up to high pressure
6	HSM down to low	0 = HSM output is not ramping down to low 1 = HSM output is ramping down to low pressure
7	HSM down to off	0 = HSM output is not ramping down to off 1 = HSM output is ramping down to off
8	unused	reads back as 0
9	unused	reads back as 0
10	unused	reads back as 0
11	unused	reads back as 0
12	J43 event	0 = inactive 1 = J43 event active
13	unused	reads back as 0
14	unused	reads back as 0
15	xhead event	0 = inactive 1 = J29 crosshead interlock (event) active

HSM off, low and high indicate that the solenoid or proportional HSM is in one of the following states, off, low or high pressure, respectively.

(0) HSM off indicates that the HSM is off, no bits are set in the HSM register.

(1) HSM low indicates that the HSM is in low pressure.

(2) HSM high indicates that the HSM is in high pressure.

(4) HSM up to low indicates that the proportional HSM in ramping up to low pressure.

(5) HSM up to high indicates that the proportional HSM in ramping up to high pressure.

(6) HSM down to low indicates that the proportional HSM is ramping down to low pressure.

(7) HSM down to off indicates that the proportional HSM is ramping down to off.

(12) The J43 event bit will be active if the switch contacts on the J43 event input are open.

(15) The xhead event bit will be set if the crosshead unlock switch connected to J29 is open. This indicates an unlocked crosshead and is traditionally used to prevent the user from going into program run.

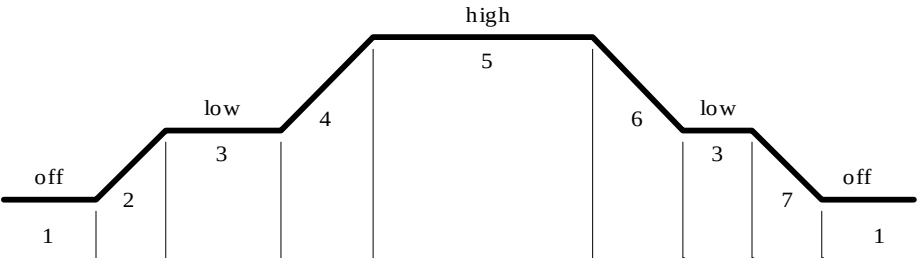
whiz bang graphical depiction of the proportional HSM status bits

The drawing below shows the typical operation of the proportional HSM. Each of the possible states is assigned an arbitrary number. These numbers are listed below each segment in the waveform and correspond to the numbers in the table, which shows when the various proportional HSM status bits are set.

Observations:

Out of the 7 status bits, only 1 bit is active at any one time.

Low pressure is the same no matter if the previous state was ramping up or ramping down.



proportional HSM status bits							
REGISTER BITS	1	2	3	4	5	6	7
off	1	0	0	0	0	0	0
up to lo	0	1	0	0	0	0	0
lo	0	0	1	0	0	0	0
up to hi	0	0	0	1	0	0	0
hi	0	0	0	0	1	0	0
down to lo	0	0	0	0	0	1	0
down to off	0	0	0	0	0	0	1

control registers

This register has all kinds of fun stuff. There is no soft dump bit on this board. To dump an entire station, use the station interlock register on the VME I/O Carrier board.

control A/B registers (addr 28, 48)

BIT	NAME	FUNCTION
0	clear intlk 1	0 = inactive 1 = clear interlocks associated with OR2-3 (HSM)
1	clear intlk 2	0 = inactive 1 = clear interlocks associated with OR1 (intlk inputs)
2	unused	reads back as 0
3	unused	reads back as 0
4	hyd enable (0)	0 = OK to write to HSM register 1 = write to HSM register will generate an interlock
5	hyd enable (1)	0 = write to HSM register will generate an interlock 1 = OK to write to HSM register
6	unused	reads back as 0
7	run / stop relay	0 = stop (relay off) 1 = run (relay on)
8	intlk override	0 = inactive 1 = interlock override active, ignore J43 intlk
9	unused	reads back as 0
10	unused	reads back as 0
11	unused	reads back as 0
12	HSM mode	0 = solenoid 1 = proportional
13	step to zero	0 = normal – prop HSM ramps on and off 1 = prop HSM steps to zero when HSM low bit cleared
14	unused	reads back as 0
15	prop HSM rate	0 = slow (approx. 4.2 sec from off to full scale) 1 = fast (approx. 2.1 sec from off to full scale)

(0-1) Information common to both clear interlock bits:

The clear interlock bits will clear the interlocks and/or events in the associated interlock or event register. Specifically, the clear interlock bits in the control A register will clear interlocks in the interlock A register and will clear events in

the event/HSM status A register. The interlocks and events for channel B will be unaffected by the channel A clear interlock bits.

These bits do not need to be cleared to 0 after writing a 1. They will always read back as a 0.

Interlocks that are common to both channels (backplane fail line, reset/power up and power fail) must be cleared separately by using both of the clear interlock bits in the channel A and channel B control registers. This prevents one SW process from clearing a common interlock that then magically disappears from the other channel's interlock register after causing a shut down.

Separate interlock bits are provided to allow separate clearing of interlocks associated with either the interlock inputs or the HSM's. These 2 resources (interlocks and HSM's) are separately mapped and could be assigned to different stations so it makes sense to have separate clear interlock bits. This feature was added in Jan-00.

(0) The clear interlock 1 bit clears the interlocks associated with an HSM channel. This is most interlocks, specifically it's the interlocks routed thru OR2 and OR3 on the interlock diagram earlier in the spec.

(1) The clear interlock 2 bit is exactly the same as the clear interlock 1 bit (above) except it clears the interlocks and events associated with the interlock inputs (on connectors J29 and J43). These are routed thru OR1 on the interlock diagram earlier in the spec.

(4, 5) The hydraulic enable bits must be set to the indicated state before writes are allowed to the HSM register. The bits are cleared back to 0's after any interlock.

(7) The run/stop bit controls the state of the run/stop relay. It is unaffected by any interlocks or events (except reset).

(8) interlock override bit – This allows the user to temporarily override an active interlock on J43. This is sometimes used to get out of a catch-22 situation where hydraulics can't be started until the interlock is cleared, but the interlock can't be cleared until hydraulics are started. A common example is an actuator that drifts down into the end cap when shut off and saturates the active conditioner, causing an interlock.

(12) The HSM mode bit controls whether the HSM output is for a solenoid HSM or a proportional HSM. Once the mode is selected, the HSM low/high bits in the HSM register are used to control either type of HSM. Changing this bit while in any state other than HSM off will probably result in unpredictable actions. Don't do it.

(13) When the step to zero bit is cleared (default mode), the proportional HSM ramps between all end levels. When this bit is set, the proportional HSM will step immediately to 0 when the HSM low bit is cleared in the HSM register. Note that this can be from either high pressure or low pressure.

To ramp from high to low, then step to off: clear the HSM high bit, wait until the HSM is in low pressure then clear the HSM low bit.

To step from high to off: clear both the HSM high and low bits at the same time.

(15) The proportional HSM rate bit allows selecting either of 2 rates for all proportional HSM ramping. Do not change this bit while ramping.

The times listed above are for a ramp from off to hi (or hi to off) without stopping in low. (This assumes that the proportional HSM high value register is set to 0xFF.) Note that this bit specifies the ramp *rate*, not the ramp *time*. If the low pressure setting is changed, the time from off to low will change, but the rate will be the same.

Precise proportional HSM ramp time calculations (traceable to the NIST)

The 8MHz clock (125nS period) is run into a 16 bit divider that is used to clock the proportional HSM state machine. An additional divide by 2 is added for the slow rate. The proportional HSM DAC is an 8 bit DAC.

Calculations for fast mode:

$$125\text{nS} * 65,536 = 8.19\text{mS per step}$$

$$8.19\text{mS} * 255 \text{ steps} = 2.09\text{S (0 to full scale)}$$

Calculations for slow mode:

$$125\text{nS} * 131,072 = 16.4\text{mS per step}$$

$$16.4\text{mS} * 255 \text{ steps} = 4.18\text{S (0 to full scale)}$$

Note that these times are for the electronics. The actual times for the ramping of the hydraulic pressure will vary somewhat from the ramp time of the electronics. This is partially due to the electronics having to ensure that the proportional solenoid is fully on and fully off at the ends of the ramp. This means that the solenoid will reach full pressure before the electronics has ramped to full scale.

HSM registers

These registers control the HSM state. All bits are R/W. The bits in this register were arranged the same as on the Europa board.

Before any writes are made to this register, other registers must be set up as described in the first few paragraphs of the *processor code* section. These paragraphs discuss clearing interlocks, etc.

These bits control both the solenoid HSM relays and the proportional HSM driver state. The HSM mode bit in the control register selects which output is active.

HSM register (addr 2A, 4A)

BIT	NAME	FUNCTION
0	unused	reads back as 0
1	unused	reads back as 0
2	unused	reads back as 0
3	unused	reads back as 0
4	HSM low	0 = output inactive, HSM off 1 = HSM in low pressure
5	HSM high	0 = output inactive 1 = HSM in high pressure
6	HSM pilot pressure	this bit is reserved for possible future use reads back as 0
7-15	unused	reads back as 0

(4) Setting the HSM low bit when in solenoid mode will energize the HSM low relay. In proportional mode it will cause the HSM DAC to ramp to the low pressure setting specified in the proportional HSM low value register.

(5) Setting the HSM high bit in solenoid mode will energize the HSM high relay. It will cause the HSM DAC to ramp to high pressure when in proportional mode.

To go to low pressure, the HSM low bit is set. To go to high pressure, both the HSM low and high bits are set. To go to off, both bits are cleared. Operation is the same in either solenoid or proportional HSM modes.

Any interlock that shuts down the HSM/station clears the HSM bits.

Refer to the *processor code* section for additional information.

proportional HSM low pressure value

This register contains the value that the proportional HSM driver will stop at when commanded to go to low pressure. The logic in the hardware will generate the proportional HSM ramp.

prop HSM low pressure register (addr 2C, 4C)

BIT	NAME	FUNCTION
0-7	low pressure	00h = off 80h = roughly half pressure FFh = full pressure
8-15	unused	reads back as 0

The state (off, low or high) of either the solenoid HSM relays or the proportional HSM driver are controlled by the HSM bits in the HSM register.

proportional HSM high pressure value

This register contains the value that the proportional HSM driver will stop at when commanded to go to high pressure. This can be useful for valves whose full scale current is substantially less than 0.7A.

prop HSM high pressure register (addr 2E, 4E)

BIT	NAME	FUNCTION
0-7	high pressure	00h = off 80h = roughly half pressure FFh = full pressure
8-15	unused	reads back as 0

Note – there is hardware checking for valid values in the proportional HSM low and high pressure registers. Illegal values will generate an interlock:

- ◆ The low pressure setting must be non-zero.
- ◆ The high setting must be greater than the low setting.

Important points on proportional HSM operation:

- ◆ Do not change the low pressure setting when in low pressure.
- ◆ Don't change the high pressure setting when in high pressure.
- ◆ Don't change either setting when ramping.

493.74 HSM board register cheat sheet

register addresses

REGISTER	CH A	CH B
board ID	00	-
intlk to station mapping	20	40
HSM to station mapping	22	42
interlock	24	44
event / HSM status	26	46
control	28	48
HSM	2A	4A
prop HSM low pressure value	2C	4C
prop HSM high pressure value	2E	4E

register bits

BIT	INTLK	EVENT / STATUS	CONTROL	HSM
ADDRESS	24, 44	26, 46	28, 48	2A, 4A
0	power fail	HSM off	clear intlk 1	-
1	-	HSM low	clear intlk 2	-
2	unconfig HSM	HSM high	-	-
3	unconfig intlk source	-	-	-
4	fail line intlk	HSM up to low	hyd enable (L)	HSM low
5	-	HSM up to hi	hyd enable (H)	HSM high
6	hyd enable fail	HSM down to low	-	HSM pilot press
7	-	HSM down to off	run / stop relay	-
8	J43 interlock	-	intlk override	-
9	-	-	-	-
10	J29 sta stop / E stop	-	-	-
11	-	-	-	-
12	prop HSM short	J43 event	HSM mode (1=prop)	-
13	illegal prop value	-	step to zero (1=step)	-
14	station interlock	-	-	-
15	reset /power up	xhead event	prop rate (1=fast)	-

x.5 processor code

This section describes common procedures for banging the bits to perform specific functions (clearing interlocks, starting hydraulics, etc.). Refer to the register/address map section for specific information on all of the individual register bits.

initial register setup

This section describes the basic registers that must be loaded by software before hydraulics can be started.

- Assign the interlock sources to a station with the channel A and B interlock station mapping registers.
- Assign the HSM's to a station with the channel A and B HSM station mapping registers.
- Set the proportional HSM low and high pressure settings for both channels (4 registers).
- Select the HSM types, either solenoid or proportional, with the HSM MODE bits in the channel A and B control registers.
- Select the proportional HSM rates in the channel A and B control registers.
- Select the proportional HSM step to zero mode as either ramp or step to zero in the channel A and B control registers.

unused channels

If the channel A HSM is used, the channel A interlock source and the channel A HSM must both be mapped to a station (the channel A interlock mapping register and the channel A HSM mapping registers must be non-zero).

Similarly, if the channel B HSM is used, the channel B interlock source and the channel B HSM must both be mapped to a station.

The interlock sources and HSM's can all be mapped to different stations. An interlock source could be mapped to an unused station if it isn't used. Any of the interlock sources or HSM's can be mapped to more than 1 station by setting multiple register bits. (The hardware wasn't intentionally designed to allow for more than 1 station line to be selected at 1 time, it just worked out that way.)

clearing interlocks

Clear interlocks only once for each press of the interlock reset button. The interlocks will need to be cleared after power up.

- Write a 1 to the CLR INTLK 1 and/or CLR INTLK 2 bits in the control register (these bits are self-clearing and don't need to be written back to a 0).
- The interlock register will be 0x0000 if all of the interlocks are cleared. If 1 or more interlocks are still active, they will be set to 1 in the interlock register.

Note that there is no lockout of interlocks in hardware. The software must keep track of which interlock occurred first. This allows the user to determine which interlock initiated the shut down when multiple interlocks become active during the shutdown. This is not a problem for the SW guys.

An active interlock has priority over the CLR INTLK bit.

starting the HSM

The HSM should be started only after the user presses the HSM low button on the pod or clicks the HSM low button on the software control panel. After an interlock, do NOT automatically clear the interlock and restart the HSM. The user must clear interlocks and then press the HSM low button again.

- Clear interlocks if necessary, see above.
- After any interlock the HYD ENABLE bits in the control register must be retwiddled. Do this by writing a 10 (binary) to the HYD ENABLE bits in the control register. Setting the HYD ENABLE bits must be done as a separate step from clearing the interlocks even though they are in the same register. This is due to timing considerations inside of the EPLD.
- Start the HPS (this is not required by the electronics, but may be required by the system).
- Set the HSM LOW bit in the HSM register.
- To switch the HSM to high pressure, set the HSM HIGH bit (leaving the LOW bit set).
- To drop back to low pressure, clear the HSM HIGH bit.
- To switch the HSM off, clear all bits in the HSM register.

Basic operation, as listed above, is the same in either solenoid or proportional HSM modes.

To ramp the proportional HSM directly from off to high pressure, set both HSM low and high bits at the same time. The circuitry will ramp to low and then continue immediately to high. As the ramp happens, the HSM status bits will show ramping to low, in low, ramping to high and then high pressure.

To ramp directly from high to off, clear both the low and high bits.

It's OK to change directions while ramping (for example, going back to off while still ramping to low).

Changing the proportional HSM low or high pressure settings will change the time between endpoints. The ramp rate is constant. For example, increasing the low pressure setting will increase the time between off and low.

Any interlock that shuts down the HSM/station clears the HSM bits.

Note – there is hardware checking for valid values in the proportional HSM low and high pressure registers. Illegal values will generate an interlock (ONLY when in proportional HSM mode):

- ◆ The low pressure setting must be non-zero.
- ◆ The high setting must be greater than the low setting.
- ◆ The HSM low bit must be set when the HSM high bit is set.

Important points on proportional HSM operation:

- ◆ Don't change the low pressure setting when in low pressure.
- ◆ Don't change the high pressure setting when in high pressure.
- ◆ Don't change the low or high pressure settings when ramping.
- ◆ Don't change the prop HSM rate bit when ramping
- ◆ Don't change the HSM mode bit (sol/prop) unless the HSM is off

When in the solenoid mode, it IS legal to set the HSM high bit and have the HSM low bit cleared. This could be useful for driving Instron or other HSM's where this is the required mode of operation. This mode is not legal when in proportional HSM mode.

It's OK to change the step to zero bit when the HSM is on.

When in proportional HSM mode the HSM low relay is energized at the beginning of the ramp and is kept on until the HSM has ramped fully to zero. The HSM high relay is switched on when the HSM is fully in high pressure.

interlock override

The user may temporarily override the J43 interlock by pressing and holding the interlock reset button.

The override bit does NOT clear any interlocks, it just blocks the action of dumping hydraulics. Any active interlocks will still show up in the interlock register.

To use override:

- Set the OVERRIDE bit in the control register.
- Start hydraulics (see above, don't forget the HYD ENABLE bits).

When done using override:

- Clear interlocks using the CLR INTLK 2 bit (this clears the individual intlk latch).
- Clear the OVERRIDE bit.

If this is done in the reverse order, or if the CLR INTLK 2 bit isn't used, the latched interlock will shut down hydraulics when the OVERRIDE bit is cleared.

support for all possible hydraulic configurations

There are non-obvious interactions between the HPS, HSM and crosshead unlock power output that tend to cause great pain and itch for the software folks.

There are 2 different types of interactions, interactions in the electronic hardware and interactions due to different combinations of hydraulic stuff.

The interactions on the electronics are due to:

- the crosshead unlock power output is the same signal as HSM high
- power for the proportional HSM circuit is switched thru the HSM low relay

This means that the HSM low and high relays need to be driven for most, if not all, hydraulic configurations.

Other than the 2 points listed above, there are no interactions lurking in the electronics. The HPS and HSM bits are really just dedicated digital I/O bits that drive relays or opto-isolators.

The interactions in the hydraulics are due to the different combinations of HPS, HSM and crosshead unlock power as listed in the table below. There are approx. 49,153 different possible configurations of the various hydraulic components (HPS, HSM and crosshead unlock power). OK, that's a slight exaggeration, but it can be a mess.

Note that the 4 lines of the table aren't the only 4 possible combinations. Any of the 3 different HPS configurations in the table can be used with any of the 4 different HSM configurations which can be used with any of the 2 different crosshead configurations.

hydraulic variables		
HPS	HSM	CROSSHEAD
none	none	none
on / off	on / off	on / off
low / high	low / high	
	proportional	

Yes, it's true that all systems must have a HPS, but not all systems have control of the HPS. Some larger labs have a centrally controlled house HPS with HSM's on each system.

On / off HPS's and HSM's use only the low bits for control (either the HPS LOW bit or the HSM LOW bit on the HSM transition board). The high bit is not used.

Observations and questions about the ramifications of this stuff:

The HSM low relay must be driven if the system is configured for a proportional HSM since the proportional HSM driver receives its power thru the HSM low relay contact. The low relay should be switched on at the start of the proportional HSM ramp up. The low relay should be switched off when the proportional HSM ramp hits zero when going to off. This will be handled by the proportional HSM circuitry on the HSM board.

The HSM high relay contact must be driven when there is high pressure to the load frame to allow the crosshead to be unlocked. This is true even if the system is configured for no HSM. This configuration has caused problems in the past, partially because systems without an HSM were frequently sold in the 1980's. This is also handled in the hardware when in proportional HSM mode.

The electronics does allow the HSM to be switched on while the HPS is left off. This may or may not be valid, but the electronics doesn't care.

If a system doesn't have an HPS, will the user have to press HPS low and high buttons before being allowed to press HSM low and high?

If a system doesn't have an HSM, how will the crosshead unlock power output get twiddled?

Instron HSM's drop the low contact when they go to high pressure. Does this need to be supported? In the solenoid HSM mode, the hardware doesn't care and the low bit may be cleared when setting the high bit.

some solutions

For upgrades to older systems without an HSM the special versions of the 493.07 will be used. They have a crosshead unlock power output that is connected to the HPS high relay in the 493.07. These are part numbers 499694-05 (24V) and -06 (115V)

Instron and other vendor upgrades will be handled with the various versions of the 493.08 interface box, which were designed specifically for this task (OK, actually for use with the very similar 493.01 chassis).

x.6 self test

None.

x.7 diagnostics

Take it away, Roy.

x.8 connections

There are 2 of each of the external connectors listed below. One set for channel A and another for channel B. Both connectors are identical except for their channel designation. Refer to the front panel view on page 3.

J28A/B HSM output CPC-4S

This is the same connector as on the 493.01 chassis – except it has both solenoid and proportional HSM outputs on the same connector (software selectable).

J28A/B HSM output		
PIN	NAME	FUNCTION
1	HSM low	24V from the HSM low relay contact
2	HSM return	return for solenoid or proportional HSM's
3	chassis gnd	for connection of cable shield
4	HSM hi/prop	either 24V from the HSM high relay contact or the output of the proportional HSM driver

J29A/B load frame D-15S

This is electrically the same connector as on the 493.01 chassis, except it uses a D connector instead of a CPC-14S connector.

J29A/B load frame

PIN	NAME	FUNCTION
1	xhead 24V	fused +24V
2	xhead intlk com	24V common
3	xhead intlk lo	low side of opto-isolator, jumpered to common
4	xhead intlk hi	hi side of opto-coupler, pulled up to 24V (opto on = intlk)
5	local E stop	local E stop loop (connect to pin 7)
6	N/C	
7	local E stop	local E stop loop (connect to pin 5)
8	HPS E stop	E stop loop from HPS (connect to pin 13)
9	N/C	
10	N/C	
11	N/C	
12	xhead unlock power	switched 24V from the HSM high relay contact
13	HPS E stop	E stop loop from HPS (connect to pin 8)
14	xhead unlock common	24V common (return for xhead unlock power, pin 12)
15	N/C	

J43A/B interlock

D-9S

This contains the same circuitry as on the 493.01 chassis except in a 9 pin D connector instead of a 15 pin connector. It is usable with either switch contacts or logic levels.

J43A/B interlock

PIN	NAME	FUNCTION
1	intlk 24V	24V thru 15k resistor
2	intlk hi	hi side of opto-isolator (opto off = intlk)
3	intlk lo	lo side of opto-coupler
4	intlk com	24V common
5	event 24V	24V thru 15k resistor
6	event hi	hi side of opto-isolator (opto off = event (soft intlk))
7	event lo	lo side of opto-coupler
8	event com	24V common
9	N/C	

J44A/B

run/stop

D-9P

Two undedicated form C relay contacts (DPDT) are available on this connector. Pin-out subject to change. Also includes opto-isolator for indicating interlock status of each station.

J44A/B run/stop

PIN	NAME	FUNCTION
1	R/S 1 NC	normally closed contact
2	R/S 1 com	common
3	R/S 1 NO	normally open contact (closed when in run)
4	intlk hi	high side of opto isolator for indicating intlk status
5	intlk lo	lo side of opto isolator
6	R/S 2 NC	normally closed contact
7	R/S 2 com	common
8	R/S 2 NO	normally open contact (closed when in run)
9	N/C	

J49A/B aux power out D-9S

Fused power for all sorts of fun projects. **Pin-out changed Apr-1-99** to add 5V. Check your cables carefully.

J49A/B aux power output		
PIN	NAME	FUNCTION
1	+15V	fused +15V
2	15V common	15V common
3	-15V	fused -15V
4	5V common	5V common
5	+5V	fused +5V
6	+15V	fused +15V
7	15V common	15V common
8	24V common	24V common
9	+24V	fused +24V

internal connectors

J1 transition bus DIN-96P

Interface to the transition bus backplane.

x.9 configuration

external jumper plugs

The following connectors require jumper plugs if no cable is installed in a system. The jumper plugs are wired the same (meaning pin numbers) as the existing jumper plugs used on the 493.01, but the connector types are different.

J29	load frame	100-007-947	3-4, 5-7, 8-13
J43	interlock	100-007-948	1-2, 3-4, 5-6, 7-8

internal jumpers and configurable stuff

There are no address select jumpers. A slot select line from the I/O Carrier board selects each board installed in the transition board backplane.

There are assorted jumpers on the run/stop relay and interlock opto-isolator drive circuits to allow them to be disconnected and jumpered to another internal signal if the need should arise. E points are provided on the HSM low and high drive circuits to allow easy connection to these points. These are provided as hooks for modifications for custom systems and are not described here. Check page 2 of the schematic for details.

There are some jumpers to disconnect the opto-isolator input on the crosshead unlock interlock (event) input. These jumpers must be in place for connecting to the traditional switch contact and removed for use with a 380 LUC (see the next section).

380 LUC (pod) interface

This board is capable of being connected to a 380 LUC for an upgrade to an existing 880/448 system. The specimen loading functions on the 380 pod are not used. The 380 pod may still be used for crosshead lock/unlock, grip lock/unlock and E stop.

The following connections are needed for 380 LUC's:

- grip intlk - closed relay contact on 380 LUC when both grips are locked. Generates program intlk when grips are unlocked. This could be routed either the event input on J43 or to one of the digital inputs. The input must then be configured in software to generate a program interlock when the contact is open.
- crosshead unlock - almost an open collector output from LUC. The opto LED on Cobra must be floating and not tied to gnd or pulled up due to the way it is driven from the LUC. The crosshead unlock interlock input on J29 must be configured for a logic level input by removing jumpers X3 and X4 for channel A or X9 and X10 for channel B. Opto on = crosshead unlocked = program intlk.

- LUC keyboard enable – this is routed to a normally closed run/stop relay contact on Cobra. This disables the LUC keyboard when Cobra is in run. The system must be in stop enable the LUC keyboard. The keyboard must be enabled to lock or unlock the crosshead or the grips.
- E stop - traditional normally closed DPST E stop switch on LUC that can be connected to the J29 load frame connector.
- power - 24V power for LUC electronics, 0.15A max. Route to the aux power connector, J49.
- crosshead unlock power - 24V output from HSM HIGH relay contact on J29 to pull in the relay in the external 24V 380 pod solenoid supply. This relay provides 24V power to the 380 LUC driven solenoids only when Cobra is in HSM HIGH pressure. This ensures that the grips and crosshead are not operated unless there is high pressure to the load frame.

The internal Cobra power supply doesn't have the current capability to drive the 380 solenoids. The existing 380 LUC 24V, 7.2A power supply (377873-01) must be used to power the 380 LUC controller solenoids (crosshead up/down/lock, grips lock and unlock, etc.).

380 LUC reference drawings:

402364-01 380 LUC functional interconnect drawing, lists all sch. numbers

561279-XX cable, 380 LUC to 493.XX Multi-channel

561343-XX mode to change 493.74 jumpers for use with 380 LUC

397190-XX cable, 380 LUC to 493.01 Cobra 1

474399-XX cable, 380 LUC to 490 TestStar Classic (old PN is 469689-XX)

x.10 why did they do that?

This section describes design details that aren't casual to the obvious observer (or something like that). This information could be useful for future modifications and fixes to the electronics. The information is organized by schematic page number.

Page 1

Nothing. This page is completely obvious to the casual observer.

Altera EPLD innards

The design of this EPLD is 100% synchronous. Except where it's asynchronous. Actually about the only things that aren't synchronous are external inputs, such as interlocks.

The EPLD logic is written in Altera AHLD. The top level design file is HSM_TRANS.TDF. The non-oblivious details are listed in the comments in the various files. Originally compiled with Altera MAX+ plus II version 9.21 running on a Win95 PC. The source files are stored on the Source Safe server.

List of Altera TDF files:

HSM_TRANS	top level file, contains all ins and outs, board ID register
HSM_REG	registers for a single channel, called twice by top level
HSM_DAC	proportional HSM DAC, called by HSM_REG
HSM_DAC_WR	writes proportional HSM values to the HSM DAC's
MUX16_1	16 to 1 mux for reading register data bits
MUX41	4 to 1 mux for reading data register bits
LOC_DTACK	DTACK state machine
DEBOUNC_R	debounce function for noisy intlk inputs

Page 2

There are pull down resistors on the inputs to the relay driver transistors to ensure that the relays are off when the outputs from the Altera EPLD are tri-stated during configuration.

Jumpers and E points are provided for disconnecting and jumpering some of the relay and opto-isolator outputs in unique combinations. This could be useful for situations where additional or custom outputs are needed. For example if a 2nd HSM low output is needed, it could be done by disconnecting one of the run/stop relays and jumpering it to the HSM low drive signal.

A place on the PWB is provided for adding a thru hole resistor for reducing the full scale output of the proportional HSM circuit. This is sometimes necessary when a lower current solenoid is used. Without an adjustment the solenoid will take a long time to start ramping down from high pressure because the standard output current is much greater than the current needed to fully open the solenoid. As an alternate, the hardware supports changing the high pressure setting by changing a register value (if the feature is implemented in software).

The proportional HSM driver transistor obtains power thru the HSM low relay contact. This is to ensure that the proportional output is off when it's supposed to be off in the event of problems with the drive transistor (oscillations, etc.).

The proportional HSM driver has a comparator circuit to monitor the current and voltage drive to the proportional solenoid. It will generate an interlock in the event of a shorted valve. This is an occasional problem if the cable is wired backwards and the driver tries to drive the forward biased snubber diode in the solenoid to 24V. The output of the comparator is heavily sedated with a large RC circuit ($t_c = 430\text{ms}$) to ignore the spikes generated when the solenoid switches to off. Note that the worst case spike isn't generated when stepping from full on to full off, it's somewhere in between.

Capacitors to ground are placed on all HSM output lines. This was done as a possible out for EMC problems, which tend to irritate signals on CPC connectors. The capacitors were found to cause occasional interlocks during testing and were removed. The problem was presumably due to large charging currents when the HSM relays switched on but was too intermittent to track down. Later ESD testing showed the same symptoms and was traced to spikes on the station interlock lines. Debounce circuits were added to the station interlock, fail and power fail inputs inside the EPLD.

Jumpers are provided on the crosshead unlock interlock input to allow use with either the usual switch contact or the somewhat unique circuitry in the 380 load frame control pod. When used with the usual switch contact, a voltage source and ground are needed. When used with the 380 LUC, the opto-isolator input must be floating. See the configuration section of this spec for more info.

2 resistors are used on the opto-isolator inputs to provided the required power dissipation for running with up to 26V on the inputs. This is a cheap and readily available alternative to pulling a new part number for a higher wattage SMD resistor.

The 24V fail detector has been deleted from the board. This function is now on the power distribution board and the power fail signal is routed on the transition bus backplane. The 24V fail interlock bit in the interlock register is now the power fail interlock bit.

The 24V fail detector was originally included because when this board was originally designed, it wasn't clear which power supplies were going to be used or if they had a reasonably priced DC fail output available.

All power supply voltages leaving the board are fused with poly fuses. These reset after an overload if they are allowed to cool for 1-2 minutes. Note that they are fairly slow to respond and are intended to protect external cabling and PWB traces.

Page 8

Jumpers are provided on the $\pm 15\text{V}$ input pins (at the transition bus connector) to allow possible operation with $\pm 12\text{V}$. This could be a desired option in the future since there has been discussion of eliminating the $\pm 15\text{V}$ supplies from the chassis to save \$\$\$\$. This mode of operation seems less likely as time goes on.

PWB and manufacturing info

The PWB is 0.062" thick FR-4 fiberglass with 4 layers: 2 power and ground planes and 2 signal layers.

Copper thickness is 2 oz. external, 1 oz. internal. Trace width is 8/8 mils.

It is mixed SMD and thru hole. Components are mounted on the both sides of the PWB.

The smallest lead pitch of all components is the Altera 10K10 EPLD, which is 0.020". All parts are flow solderable and washable.

x.11 timing diagrams

None.

x.12 list of related drawings

493.74 HSM board part numbers

PART NUMBER	DESCRIPTION
560863-01, -02	top level assemblies (channels 1-2, ch. 3-4)
700-000-291	board schematic
100-009-026	PWB
100-009-028	circuit board assembly
100-010-954	programmed Altera EPLD config PROM
100-004-258	blank Altera EPLD config PROM (EPC1441)
100-000-656	Cobra MC cable selector drawing
100-000-654	Cobra MC setup / config drawing
XR-2200	muffler bracket for '79 Pinto*

* *Airplane II*, 1982, Paramount Pictures